

JADE

Computer Products

DOUBLE D

DOUBLE DENSITY DISK CONTROLLER

DOUBLE DENSITY DISK CONTROLLER WITH ON-BOARD Z-80

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NOTICE

The following corrections should be made to the hardware manual.

1. PAGE 24 - C41 (4.7 uf 25 volt) tantalum is to be installed in reverse of silk screen.
2. APPENDIX A - Change polarity of C41 in component layout diagram. It is near IC 4B.
3. APPENDIX E - Change polarity of C41 in component layout diagram. Add to correction list ITEM #6

"C41 polarity is reversed in silkscreen."

In some kits C32 and C41 are 4.7 uf 20 volt. This substitution is approved. In some kits C32 and C41 tantalums are color banded (Yellow-Purple-Grey). When installed at C32 the white strip faces J4. When installed at C41 the white strip faces the S100 connector.

JADE COMPUTER PRODUCTS

PRESENTS

Double D

THE DOUBLE DENSITY DISK CONTROLLER

HARDWARE MANUAL

IOD-1200M

REVISION B

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SECTION 1

INTRODUCTION

1.1 SCOPE

This manual contains the complete hardware description of the Jade Double Density Disk Controller. It provides the end user with construction and configuration procedures, and a functional description of the circuitry.

1.2 RELATED DOCUMENTATION

Double D Software Manual P/N IOD-1201M
FD 179X-01 Specifications
Z80A-CPU Technical Manual

Jade Computer Products
Western Digital Corp.
Zilog, Inc.

1.3 DESCRIPTION

The Double D is an intelligent S-100 based disk controller. It is capable of handling up to four full size (8") or mini (5") disk drives. Provisions have been made for double sided drives. Single and double sided drives may be mixed. The controller is capable of single density (FM) and double density (MFM) operation. It can be used in software polled as well as interrupt driven environments. Circuitry is implemented on a four layer printed circuit board where one inside layer is used entirely as a ground plane. This provides for a minimal amount of ground noise. This board was designed to meet the proposed S-100 signal disciplines as defined in IEEE Task 696.1/D2

The Double D contains an on-board Z80A microprocessor with 2K of static memory. The on-board processor runs simultaneously with and transparent to the S-100 bus. All critical timing is handled on-board; data transfers are fully buffered by sector in the on-board memory, two levels of interrupt are implemented on the Z80A, and a wait state generator is used to synchronize the on-board processor to the disk transfer rate. The host system (8080, 8085, Z80, or ?) need only transfer commands and data through a block of static memory, which can be accessed from the bus. This architecture provides a high degree of timing independence from the host system. Also, since the disk controller program is contained on-board in ram, this board's operational characteristics are redefinable at any time during system operation.

The powerful WD 1791-01 Formatter/Controller is used to encode and decode all data transfers to and from the disk drives. It also provides for the generation and checking of address marks, data marks, and the cyclic redundancy characters. Write Precompensation can be selected under software control at three levels of intensity, providing flexible data recording. Data separation is achieved by the use of a phase-locked loop to insure maximum immunity to disk speed variation and to enhance data recovery margins in both single and double density.

1.3 DEVICE SPECIFICATION

Power requirements:	+7 TO +11 Volts	0.90 Amp. Typical 1.50 Amp. Maximum
	+14.5 to +21.5 volts	25 Ma. Typical 50 Ma. Maximum
	-14.5 to -21.5 volts	8 Ma. Typical 30 Ma. Maximum
System Port Requirement:	One I/O port, switch selectable	40,41,42,43 Hex
System Memory Requirement:	1K Byte block, switch selectable	E400,EC00,F400,FC00 Hex
	with optional jumper switch selectable	E000,E800,F000,F800 Hex
Recording Method:	Single density in FM Double density in MFM	
External Communication:	One EIA level input signal One EIA level output signal	
Disk Interface, Connectors:	8" Drives	50 Pin Card Edge Connector AMP P/N 888083-1 3M P/N 3415-0001
	5" Drives	34 Pin Card Edge Connector AMP P/N 583717-5 3M P/N 3463-0001
System Interrupts:	Optional Feature, Vector Interrupt on	VIO* thru VI7*

SECTION 2

HARDWARE DESCRIPTION

2.1 OVERVIEW

The operational characteristics of the DOUBLE D are a function of both hardware and on-board software. The hardware provides the data paths, logic functions, and control signals necessary to implement such operations as head loading, drive selection, head positioning, and transferring data. It is the software that determines how the disk controller commands are interpreted and in what sequence controller events take place. As in all microprocessor designs, the software can do no more than hardware implementation allows. The DOUBLE D is designed to allow the on-board software as much control as possible. For the user who will write control programs for this board, an understanding of the hardware is recommended. This section provides a description of the hardware.

2.2 MEMORY ADDRESS DECODING

The S-100 bus address lines are constantly monitored by the Memory Address Detection circuit. See Figure 2-1. In the Standard address mode, ICs 3H and 3B implement detection of the selected 1K memory block. Switches M11, M12 and optional jumper MA10 are used to locate the selected memory block on any 1K boundary from E000 to FC00. Note: signals SA11 and SA12 indicate the corresponding address switch settings. See Table 2-1. For the Extended Address Mode, IC 4B must be installed and the Address Mode Block altered to the appropriate position. In this configuration, address decoding is provided for any 1K block in the upper 8K in the 24 bit address bus. In either mode, an address match is indicated by BMA* (Bus - Memory Addressed) being asserted (low).

SWITCH M12	SWITCH M11	SA12	SA11	ADDRESS RANGE WITH MA10	ADDRESS RANGE WITHOUT MA10
Close	Close	0	0	E000 - E3FF	E400 - E7FF
Close	Open	0	1	E800 - EBFF	EC00 - EFFF
Open	Close	1	0	F000 - F3FF	F400 - F7FF
Open	Open	1	1	F800 - FBFF	FC00 - FFFF

Table 2-1. Memory Address Selection

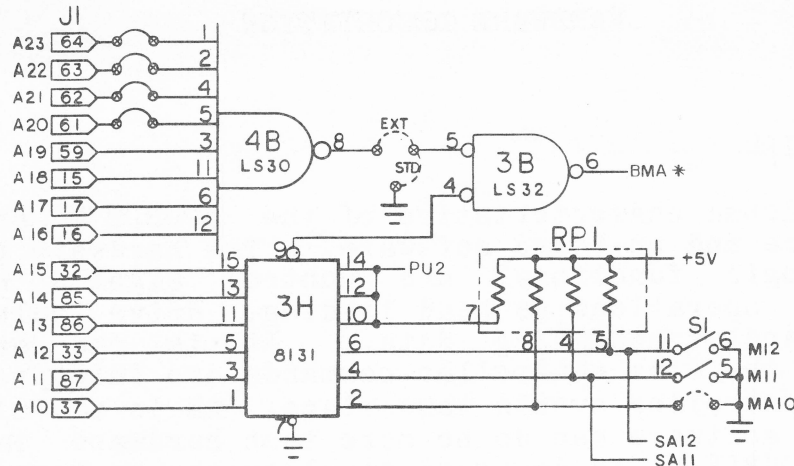
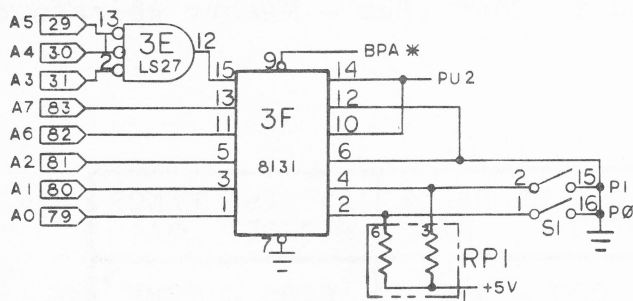


Figure 2-1. Memory Address Detection

2.3 PORT ADDRESS DETECTION

S-100 address lines A0 thru A7 are constantly monitored by the Port Address Detection circuit. This circuit is composed of IC 3F and part of 3E. See figure 2-2. Switches "P0" and "P1" are used to vary the selected port address from 40 thru 43 hex. An address match is indicated by BPA* (Bus - Port Addressed) being asserted.

Figure 2-2.
Port Address Detection

SWITCH P1	SWITCH P0	ADDRESS PORT
Close	Close	40
Close	Open	41
Open	Close	42
Open	Open	43

Table 2-2.
Port Address Selection

2.4 BUS CONTROL SIGNALS

All Control Signals from the S100 bus are buffered by ICs 1H and 3K before internal use. These line receivers have schmitt trigger inputs typically offering 400 millivolts hysteresis. See Figure 2-2.

In some older mainframes SLVCLR* is not implemented. For use in those systems POC* (pin 99) can be connected to SLVCLR* by a jumper.

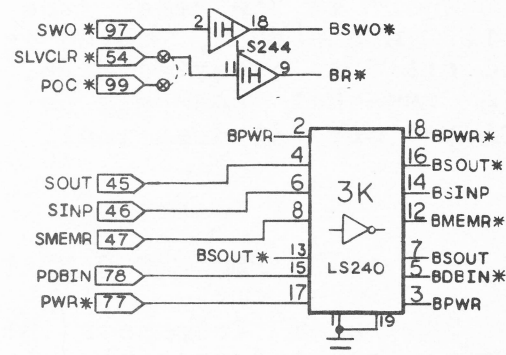


Figure 2-3.
Control Signal Buffers

2.5 DISK PROCESSOR CONTROL PORT

The Disk Processor Control Port is an S-100 output port which provides the host system with control of the on-board processor. The port is strobed by the occurrence of sOUT, pWR*, and a matching port address (BPA*). The following functions are implemented.

1. Switch internal memory to and from the bus.
2. Issue an interrupt to the Z80A processor
3. Reset the Z80A processor.

The board reset signal BR* brings the port to the initial state where internal memory is switched into the S-100 bus. Refer to Figure 2-4 for circuit details.

SLVRQ is set by data bit 0. Asserting SLVREQ* initiates the memory switch process. SLVRQ* is applied to the Z80A BUSREQ* pin. When SLVRQ* (BUSREQ*) is asserted, the Z80A tri-states its data, address, and control lines. The Z80A then asserts SLVACK* (BUSACK*). Refer to the Z80A TECHNICAL MANUAL. Assertion of SLVACK* enables the Memory Control circuit to respond to S-100 memory cycles.

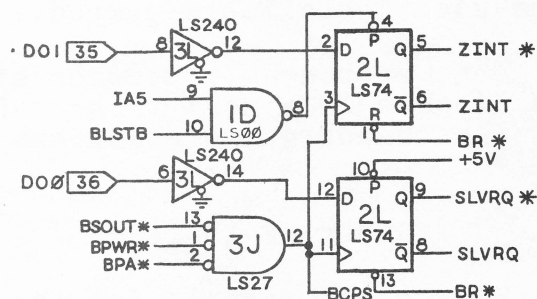


Figure 2-4.
Control Port

ZINT is set by data bit 1. ZINT(*) serves a dual function. ZINT* is the maskable interrupt request to the on-board Z80A. Note, circuit implementation makes it possible for the on-board Z80A to test and reset ZINT* under software control. More on this later. ZINT also controls which 1K bank of internal memory is selected for bus access. When memory is switched to the S-100 bus, the on-board Z80A has asserted SLVACK* and will not respond to an interrupt. At this time ZINT is used as internal address bit 10.

ZRST* is the reset line to the on-board Z80A. It is an output of IC 1A, a one-shot, which is triggered by writing to this port while data bit 7 is asserted high. Due to the gating of IC 3B (See pin 12) this one-shot can only be triggered when the on-board Z80A is in BUSACK* (SLVACK* asserted).

2.6 DISK PROCESSOR STATUS PORT

The Disk Processor Status Port is an S-100 input port which allows the host processor to examine the current state of the Disk Processor. The port responds to the occurrence of pDBIN, sINP, and a matching port address (BPA* asserted). The following states can be determined by reading this port.

1. On-board memory accessibility from the bus.
2. On-board processor state (Run/Halt)
3. Address of the 1K memory window.

Presence of the memory window is indicated when reading SLVACK*. This signal corresponds to data bit 0. Reading a "0" indicates that the memory window is present. The address of the memory window is determined by reading the M11 and M12 switch positions as indicated by signals SA11 and SA12. SA11 corresponds to data bit 2 and SA12 corresponds to data bit 3. Table 2-1 shows the relation between SA11-SA12 and the selected window address. MA10 is an user installable jumped.

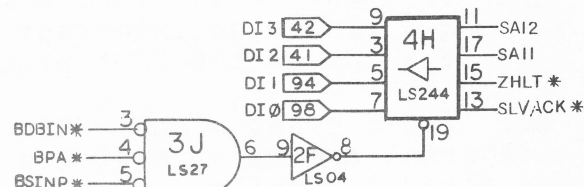


Figure 2-5.
Processor Status Port

The on-board processor state is indicated when reading ZHLT*. This is the Z80A halt flag. Reading a "0" on data bit 1 indicates that the on-board processor has halted.

2.7 CLOCK GENERATION

The clock signals for the Z80A and WD 1791-01 are generated on-board by a crystal oscillator, divider and driver. See figure 2-6. The crystal is a fundamental type operating at 8.000 Mhz. The oscillator is implemented with two sections of IC 3L. A third section is used to square the output of the oscillator. IC 2M is used to divide the clock. The CLOCK SELECT JUMPER is set depending on the disk drive to be used. The WD 1791-01 requires a 2.000 Mhz clock for 8" drives and a 1.000 Mhz clock for the 5" drives. The jumper provides for the selection of a additional divide by 2. With 8" drives the Z80A is run at 4.000 Mhz. With 5" drives the Z80A runs at 2.000 Mhz to provide adequate port enable (RE* and WE*) timing for the WD 1791-01. A section of IC 1E and U-5 provide a MOS level clock driver for the Z80A as recommended by Zilog.

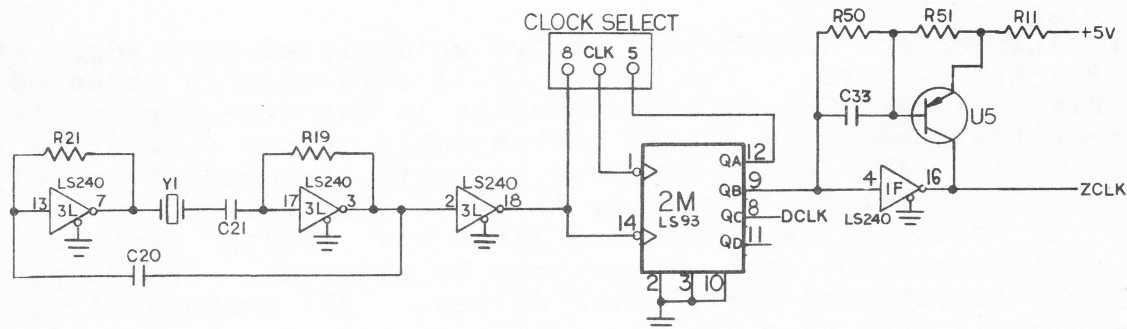


Figure 2-6. Clock Circuit

2.8 PROCESSOR

The on-board processor function is implemented with the Z80A. It was selected because of execution speed and compatability with TTL logic families. The processor uses the on-board 2K static memory for program, stack, parameters, and for buffering single/multiple sectors of data. Because the 5 upper address bits are not decoded, this 2K block appears 32 times in the Z80A 64K address range. This allows internal programs to be assembled on any 2K boundary. Note, the address selected for the memory window has no effect on the on-board processor or the on-board software.

The host system communicates with the on-board processor thru the memory window. During a system boot, the control program must be loaded thru the memory window before the on-board processor can operate properly. It is entirely possible for the initial control program to be a small bootstrap which then loads a larger control program from disk. For reading and writing disk sectors, the host system must block move sector data through the memory window.

Both Z80A interrupts are implemented. The host system issues the maskable interrupt by executing an OUTPUT instruction to the Disk Processor Control Port. The WD 1791-01 issues an interrupt upon command completion. The Z80A NMI* pin is used for interrupts from the 1791-01. This interrupt is clamped by CR18 when DSE (Drive Select Enable) is low.

2.9 DISK CONTROLLER

The Western Digital 1791-01 is used for all data transfers to and from disk. This device is addressed as four I/O ports from the on-board processor. The user should refer to WD 1791-01 specifications for a detailed description of this part. Access to the WD 1791-01 Status Port allows reading the disk interface signals. These are WRITE PROTECT*, READY*, INDEX*, TRACK-ZERO*, and SEEK-COMplete*.

2.10 DISK INTERFACE

Disk Interface is provided by two gold-plated card edges at the top of the P.C. board. The 50 pin (J-3) card edge is intended for the 8" disk drives. The mating connector is the same type as is used to connect the other side of the ribbon cable to the disk drive (with most drives). All even numbered contacts (component side) are connected to internal circuitry thru a double set of plate-thru-holes. By cutting the connecting links and adding jumpers, the signal assignments for each contact can be altered. The 34 pin card edge (J-2) is intended for 5" disk drives. All unassigned contacts provide a plate-thru-hole for alteration. Additional signals can be assigned to this connector by jumping from J-3 to J-2. On connectors J-2 and J-3 all odd-numbered contacts are grounded.

2.11 INTERNAL I/O ADDRESSES

There are seven I/O ports available to the on-board processor. These internal ports are not accessible from the host system. They are used for control signals, status information, and data paths. They are decoded using address bits A0 thru A2.

ADDR	TYPE	DESCRIPTION
00	Input	Board Level Status
00	Output	Board Level Command
04	Input	Disk Controller Status
04	Output	Disk Controller Command
05	I/O	Disk Controller Track
06	I/O	Disk Controller Sector
07	I/O	Disk Controller Data

Table 2-3. Internal I/O Ports

Address bits A3 thru A7 have no effect on I/O operations except when accessing the Board Level Status Port. These upper address bits individually trigger on-board events when asserted high during an INPUT operation from this port. A list is provided in Table 2-4. For a detailed description refer to the appropriate section.

BIT	FUNCTION	SECTION
A3	Issue Step Pulse	2.15
A4	Clear Timer	2.14
A5	Reset Host Interrupt	2.5
A6	Initiate Timer	2.14
A7	Wait State Request	2.16

Table 2-4. Address Bit Assignments

2.12 BOARD LEVEL STATUS PORT

The Board Level Status Port is a parallel input port to the on-board Z80A. It provides the processor with access to board signals that cannot be read from the WD 1791-01. These signals are listed and described in Table 2-5. See Figure 2-7 for circuit diagram.

DATA BIT	SIGNAL NAME	DESCRIPTION
0	R0	R0 switch setting.
1	R1	R1 switch setting
2	TST*	Test mode
3	ZINT	Interrupt req from host
4	SERI	EIA level input bit
5	TOFF	Timer off
6	ILP*	Illegal pack inserted
7	CHNG*	Disk has been changed

Table 2-5. Board Level Status Bits

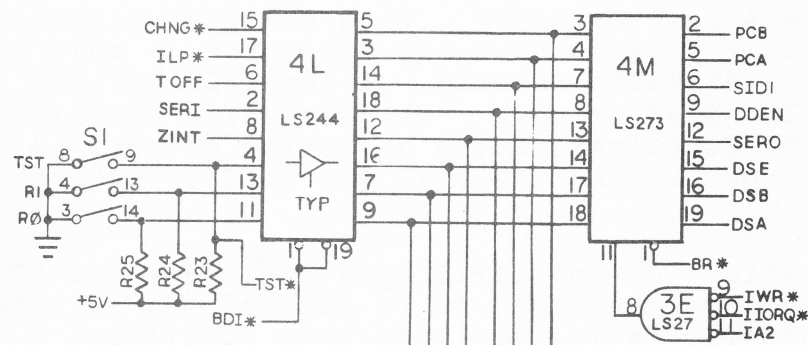


Figure 2-7. Board Level Ports

2.13 BOARD LEVEL COMMAND PORT

The Board Level Command Port is a parallel output port of the on-board processor. It is used to select various parameters as listed in Table 2-6. See Figure 2-7 for circuit details.

DATA BIT	SIGNAL NAME	DESCRIPTION
0	DSA	Drive select bit A (2**0)
1	DSB	Drive select bit B (2**1)
2	DSE	Drive select enable
3	SERO	EIA signal output control
4	DDEN	Double density enable
5	SID1	Side and direction select
6	PCA	Precomp select A
7	PCB	Precomp select B

Table 2-6. Command Port Bits

The signals DSA and DSB are used to determine which drive is selected. DSE must be asserted for drive selection to take place. DSE is also used to enable the on-board processor to accept an interrupt from the 1791-01. See Table 2-7 for drive selection.

DSE	DSB	DSA	DRIVE
0	X	X	NONE
1	0	0	0
1	0	1	1
1	1	0	2
1	1	1	3

Double Density operation is enabled when DDEN is set high. A low SERO signal corresponds with a negative EIA output.

Table 2-7.
Drive Selection

SID1 serves a dual function. When using double-sided drives and performing any type of read or write operation, this signal selects which side of the diskette is used. A low SID1 selects the same side as used on single-sided drives. When stepping operations are being performed, SID1 functions as the direction select, a low SID1 will cause stepping operations to move the head toward track 0 (most drives).

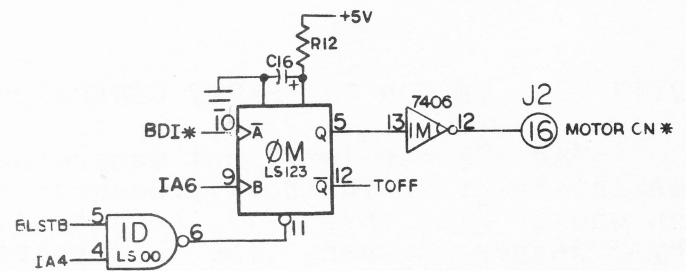
Precompensation is controlled by signals PCA and PCB. These two signals allow precompensation to be enabled and at three different levels of intensity. Table 2-8 lists this function.

PCB	PCA	PRECOMPENSATION
0	0	OFF
0	1	200 ns.
1	0	160 ns.
1	1	120 ns.

Table 2-8. Write Precompensation

2.14 ON-BOARD TIMER

The On-Board Timer provides both a motor control for 5" drives and a means for deselecting any drive if not used for a given period of time. The 1791-01 will unload the head of a drive if not used in 15 revolutions, but in some drives the stepper-motor will still consume power. The timer is under complete control of the on-board processor. It can be set, reset, and examined by appropriate I/O operations. See figure 2-8.

Figure 2-8.
On-board Timer

2.15 STEP CONTROL

The STEP CONTROL circuit provides more flexible control of the step function than the 1791-01. Step pulses are issued under control of the on-board processor. The interval between step pulses are timed by on-board software and can be resolved to better than 0.10 milliseconds. The step pulse width has been set at 3 microseconds. This appears satisfactory for most disk drives. If needed, this value can be altered by choosing a new value for C9 or R10. See Figure 2-9.

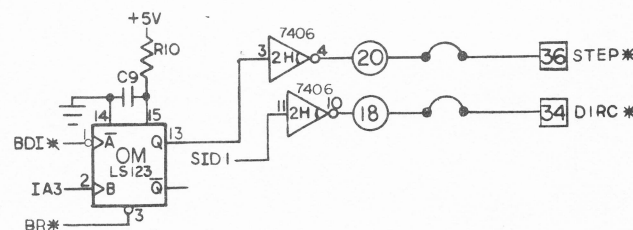


Figure 2-9. Step and Direction

2.16 WAIT STATE GENERATOR

The Wait State Generator is used to synchronize the on-board processor to the Disk Controller when data is being transferred between the Double-D and a disk drive. The wait state is generated during the execution of an input instruction from the Board Level Status Port while address bit A7 is held high. The wait-state is held until the WD 1791-01 issues either a Data Request (DDRQ) or an interrupt (DINT). For circuit details refer to figure 2-10.

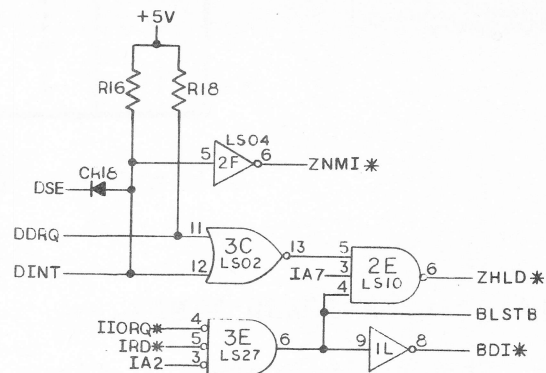


Figure 2-10. Wait States

2.17 VECTOR INTERRUPT GENERATOR

The Vector Interrupt Generator may optionally be used to issue an interrupt to the host processor system. The interrupt is issued on one of VIO* thru VI7*, selectable by jumper, when the on-board processor executes the HALT instruction. The interrupt request is terminated when the host processor either switches the Double-D memory into the S100 bus or issues an interrupt to the Double-D. See figure 2-11 for circuit details.

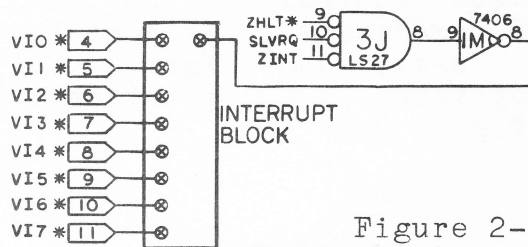


Figure 2-11. Vector Interrupts

2.18 EIA LEVEL INTERFACE

The EIA LEVEL INTERFACE provides the level conversions to and from TTL. These EIA level lines are made available at connector J4, an 8-pin DIP socket located close to IC 1A.

2.19 MEMORY CONTROL

The Memory Control Circuit is used to operate the on-board memory. When SLVACK* is high, the on-board Z80A is performing memory read and write operations. When the internal memory is present in the S100 bus (SLVACK* low), the host processor may perform read and write operations. Refer to Figure 2-12 for circuit diagram.

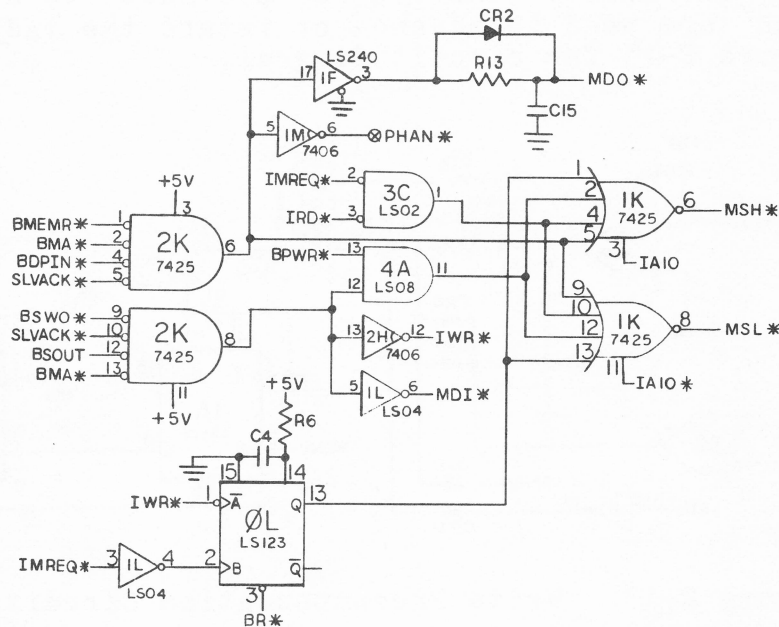


Figure 2-12. Memory Control Circuit

S100 bus requests for read and write operations are decoded by IC 2K. IC 2K pin 6, when high, indicates a memory read is taking place. IC 1M pin 6 can be used to provide PHANTOM* to the S100 bus to avoid a bus driver conflict when using memory cards which overlap the selected memory window address. Many 64k dynamic RAMs cannot dissable 1K segments. IC 1F pin 3 is used to enable the data out driver, IC 4J. R13 and C15 provide approximately 120 ns. turn-on delay, allowing PHANTOM* enough time to turn any other memory off. IC 2H pin 8 indicates a bus write is about to take place. This signal pulls IWR* down indicating to the 2114's that this is a write cycle. MDI* is also asserted, which enables the data-in buffer (IC 4K). When pWR* is asserted IC 4A pin 11 goes high. Either pin 6 or 8 of IC 1K then enables a bank of 2114. The memory bank selected is determined by IA10 and IA10* applied to pins 3 and 11 of IC 1K.

IC 3C detects the on-board processor read cycle. IC 1K again provides the bank enable signal. An on-board processor write cycle is detected by one-shot OL (IWR* and IMREQ*). The output OL pin 13 is used to strobe the appropriate bank enable (through IC 1K). During this strobe IWR* is held low, indicating a write cycle for the 2114s.

2.20 WRITE PRECOMPENSATION

The Write Precompensation circuit is used advance or retard the individual write data pulses. This is done to correct for a distortion called BIT SHIFT. This bit shift is observed when reading a data stream from a diskette. Data pulses which are recorded close together, when read back, appear to spread apart. This circuit shifts the pulses being recorded in the direction opposite of the direction of this bit shift. The 1791-01 provides two signals, EARLY and LATE, which are used to advance or retard the individual data pulses. See Figure 2-13 for circuit diagram.

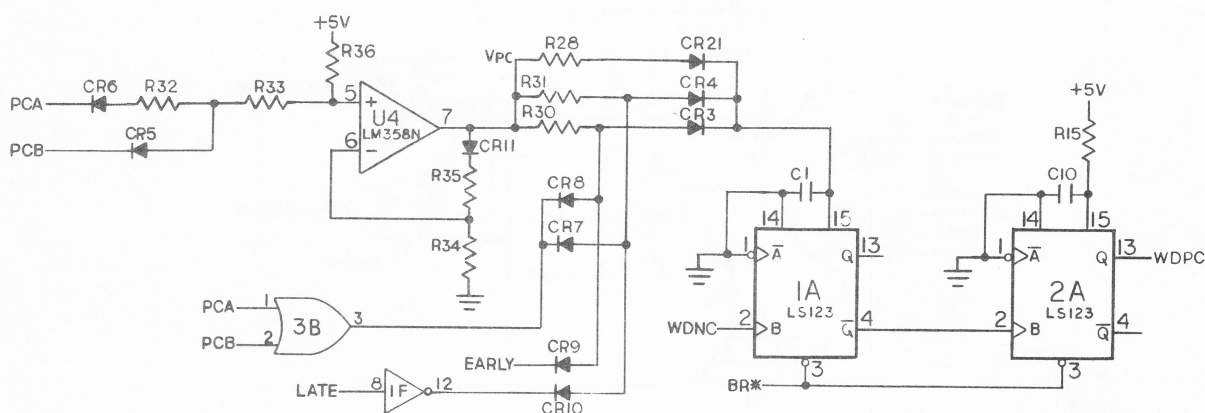


Figure 2-13. Write Precompensation Circuit

Signals PCA and PCB are used to produce three different voltage levels at U4 pin 5. This level is amplified by U4 and then used as the pull-up voltage source for one-shot 1A. R30 and R31 are individually switched by EARLY and LATE to vary the one-shot period. R28 is always in circuit. It determines the longest period. When neither EARLY nor LATE are applied, R28 and R31 in parallel determine the period. With EARLY asserted, R30 is included in parallel to provide the shortest period. The amount of precompensation applied is the difference between the normal period and either the short period or the long period. By selecting the voltage applied to the pull-up resistors, the amount of precompensation is varied. IC 3B is used to inhibit precompensation when PCA and PCB are both low.

2.21 PHASE-LOCKED LOOP

A Phased-Locked Loop is used to generate the read clock as required by the 1791-01 for data separation. This method was selected as it provides maximum immunity to disk speed variation and provides enhanced data recovery margins in both single and double density. The loop is constructed of both digital and analog circuitry.

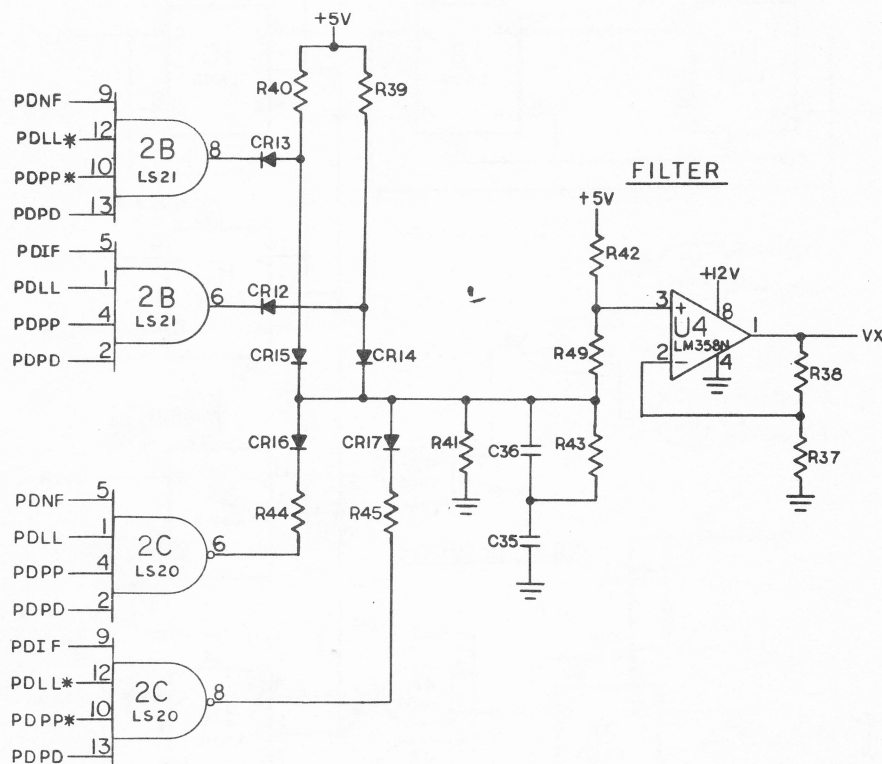


Figure 2-14. Phase Detector and Filter

The Voltage Controlled Oscillator (VCO) is a 74LS123 with both sections configured to trigger each other. The control voltage is applied to the resistors R3 and R4/5. An increase in voltage corresponds to an increase in frequency. IC 2A, a section of a 74LS123, also uses VX to provide this one-shot with a period which proportionally tracks the period of the VCO. See Figures 2-14 and 2-15.

A set of timing signals are generated from the VCO which are used by the Digital Phase Detector. IC's 1C and 3A are 74LS113s and are used to generate these signals. They are all clocked simultaneously to eliminate any skew in the generated signals.

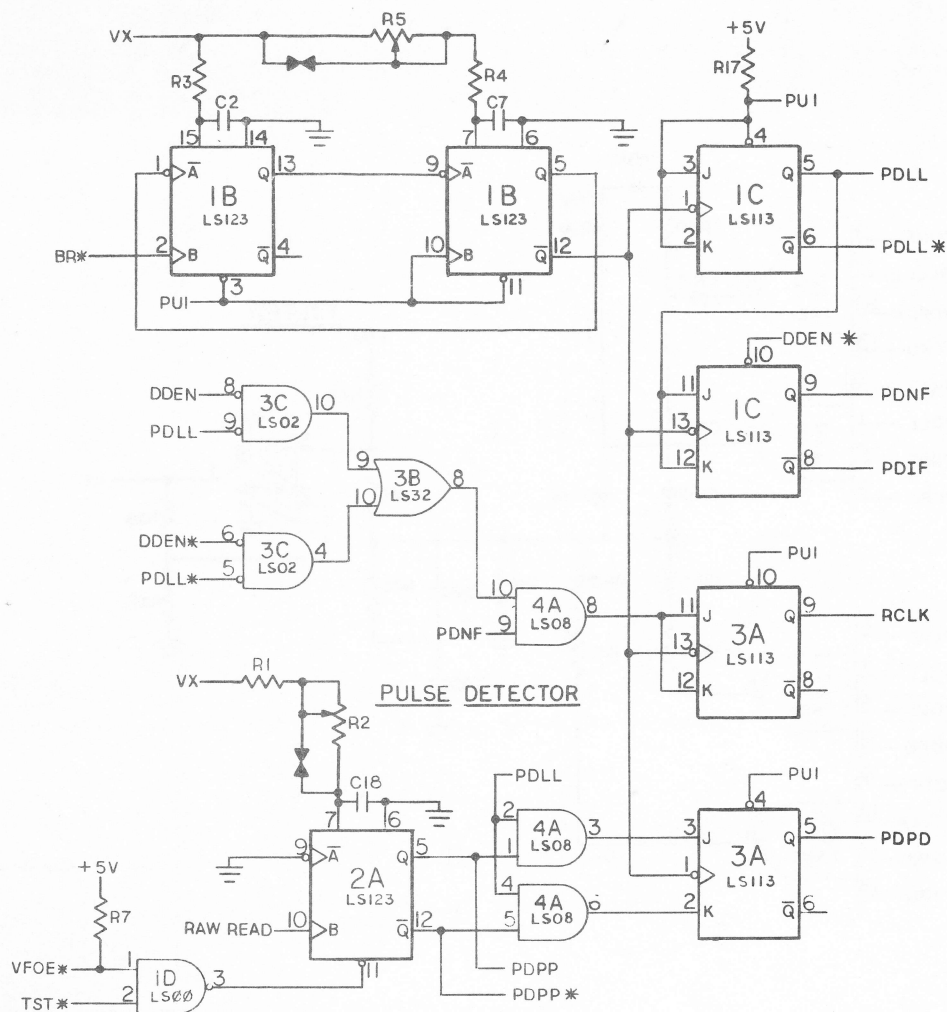


Figure 2-15. VCO and Timing Generator

In the following discussion 8 inch operation is assumed (With 5 inch operation all timings are doubled). In double density (MFM), the incoming data stream contains bits which are separated by 2, 3, or 4 microseconds (wishful thinking!). Read Clock makes a transition every 1 us. The Phase-Locked Loop adjusts the VCO such that each data pulse is centered in the middle of a half-cycle of Read Clock (Window). More precisely, due to bit-shift, very few individual data pulses are centered. They tend to occur either a little early or late but the center of the spread in these pulses is centered in the window.

The signal PDLL (Phase Detector Lead/Lag) divides the window into early and late sections. PDNF (Phase Detector Normal Frame) is always true in double density. Its complement PDIF (Phase Detector Illegal Frame) is used in single density only. In single density, when the data pulses are separated by either 2 or 4 microseconds, every other 1 us frame of the phase detector is an Illegal Frame for single density operation. RCLK (Read Clock) is generated for both FM and MFM. Sections of ICs 3C, 3B, and 4A provide this switching

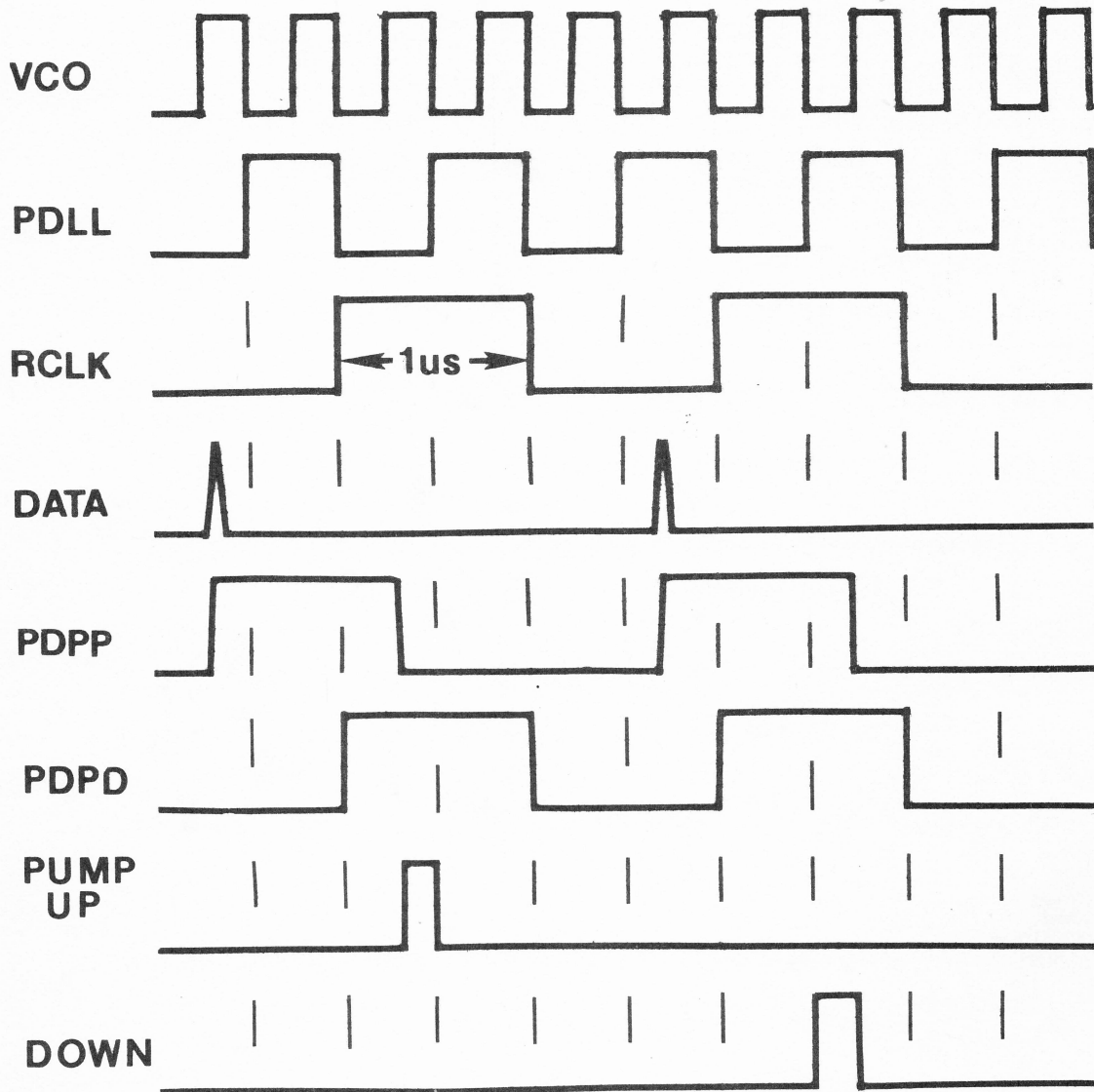
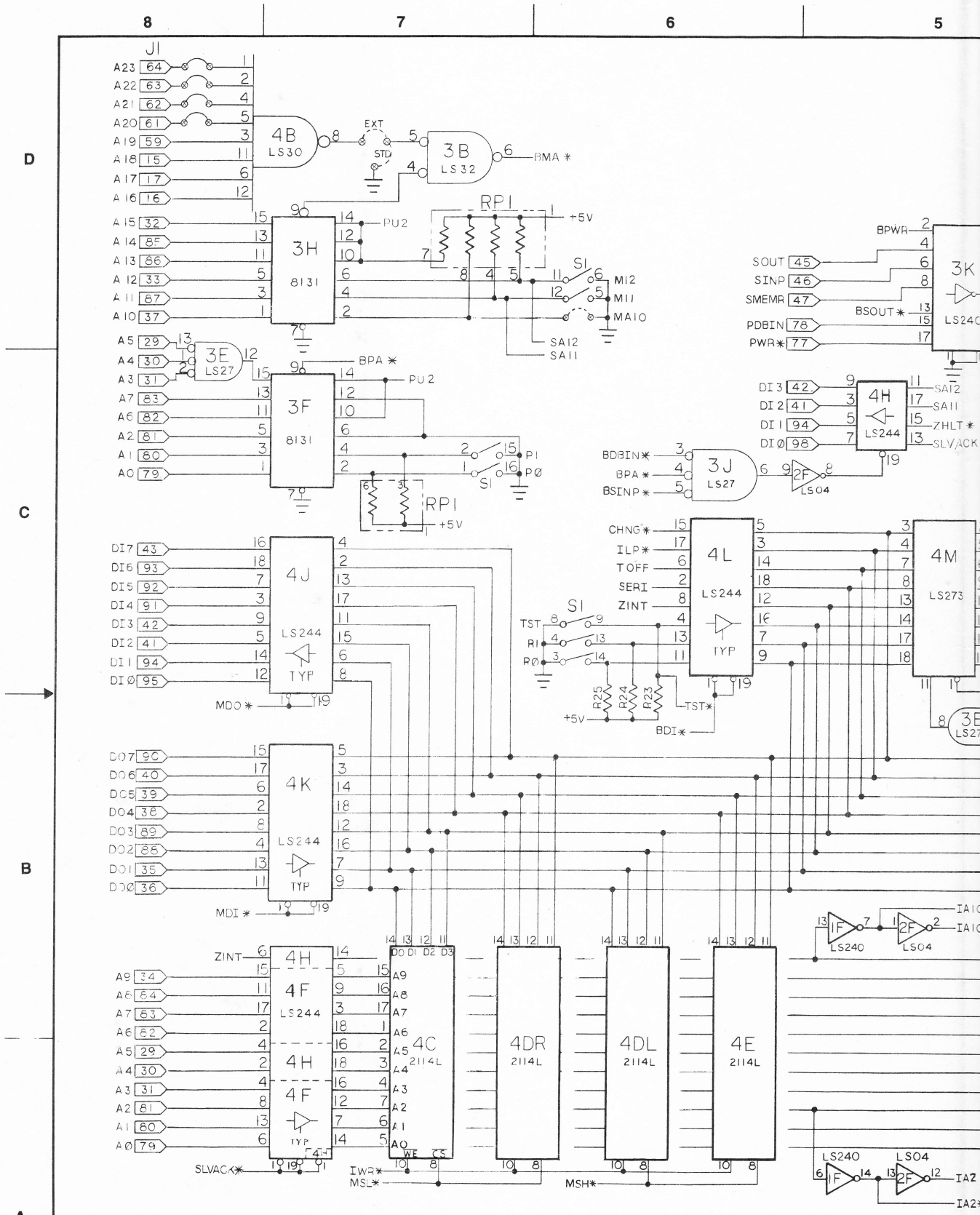


Figure 2-16. 8 Inch MFM Operation

logic. PDPD (Phase Detector Pulse Detected) indicates that during the last 1 us frame a data pulse was detected. This signal is maintained during the entire frame. PDPP (Phase Detector Pulse Present) is the output of a one-shot with a period of 1 us. It is triggered by an incoming data pulse. The falling edge of this signal occurs at the same place in the next frame as the data pulse occurred that triggered the signal in the preceding frame.

All these signals are used by the Phase Comparator which adjusts VX. The comparator provides Pump Up and Pump Down signals, where the period of the pump pulse is the same as the deviation of the incoming data pulse from the window's center. See Figure 2-15. This figure shows the internal phase signals, an early and late data pulse, and the corresponding pump pulses.



SYMBOLS

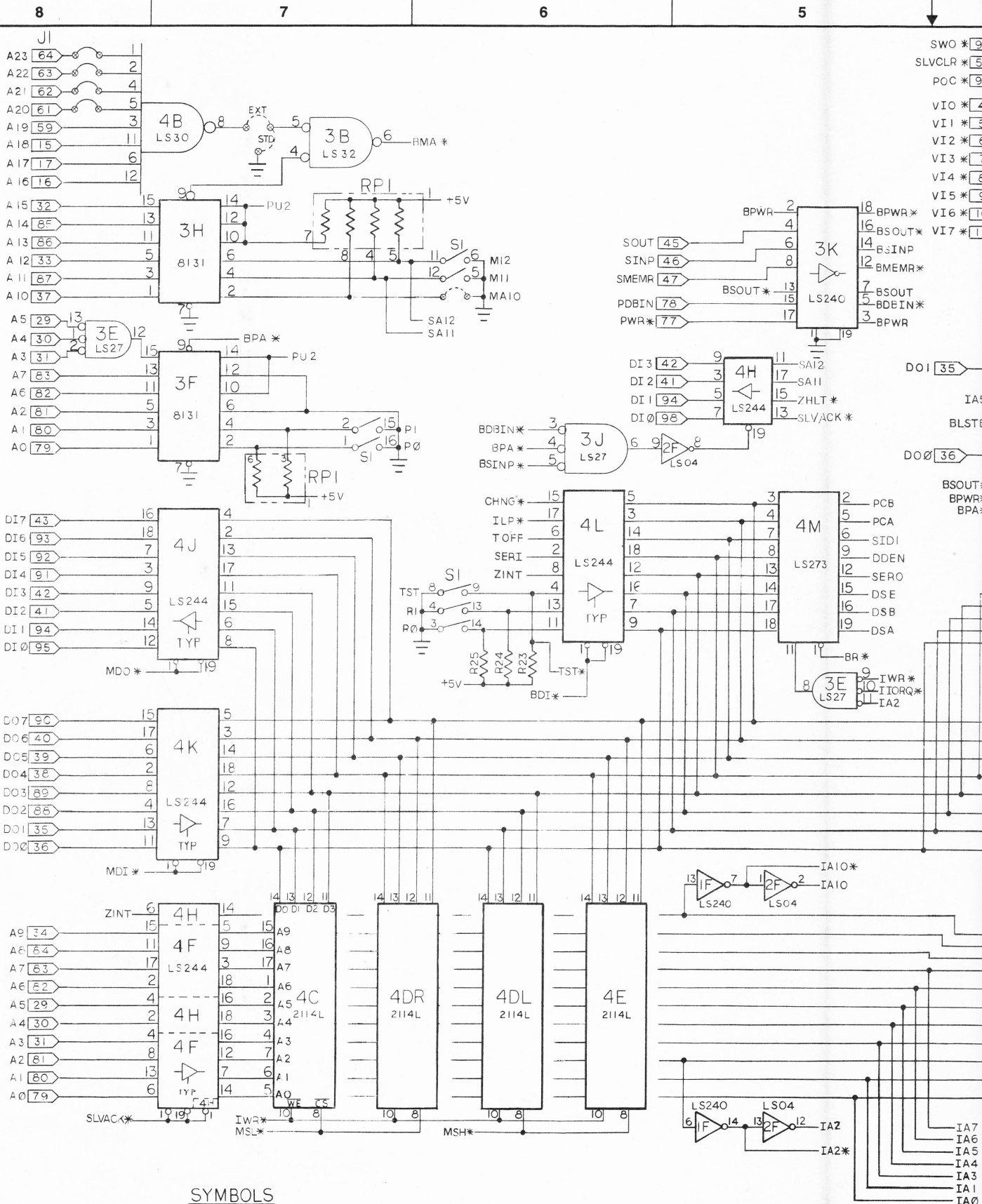
- ⊗ PLATED THRU HOLE
- Ⓢ TERMINATOR
- ⊕ OPTIONAL JUMPER FACTORY INSTALLED
- ⊖ OPTIONAL JUMPER USER INSTALLED
- ⬇ FOIL USER CUT

D

C

B

A

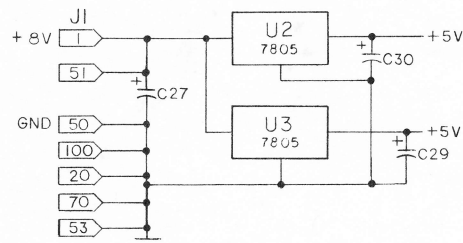


SYMBOLS

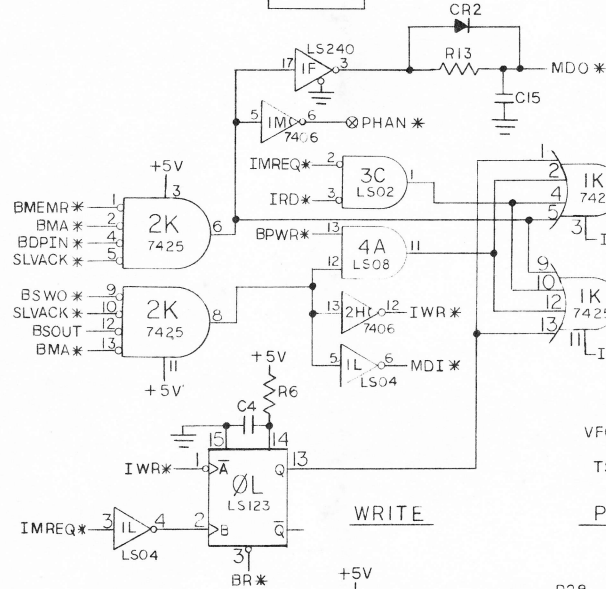
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- Ⓢ TERMINATOR
- ⊕ OPTIONAL JUMPER FACTORY INSTALLED
- ⊖ OPTIONAL JUMPER USER INSTALLED
- ⬄ FOIL USER CUT

D

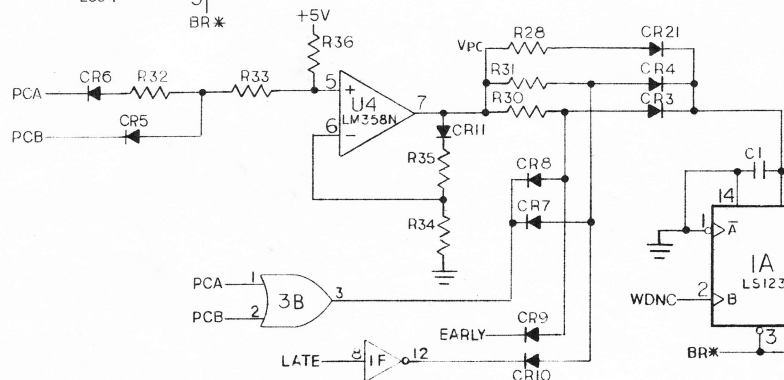
VOLTAGE REGULATORS



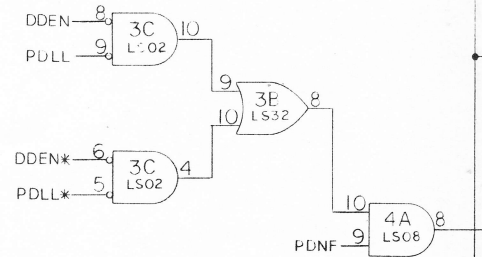
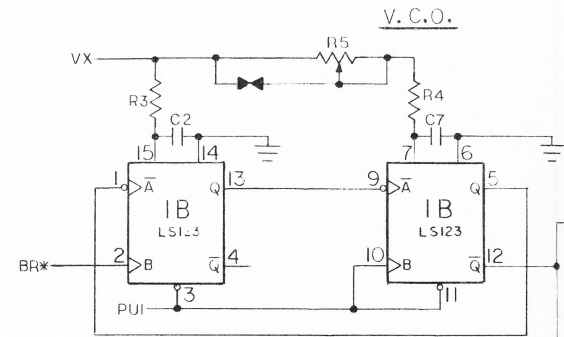
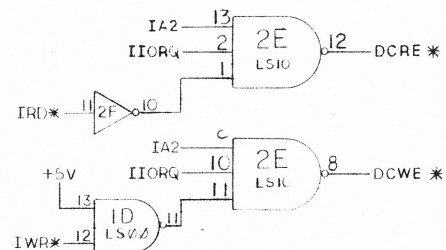
C



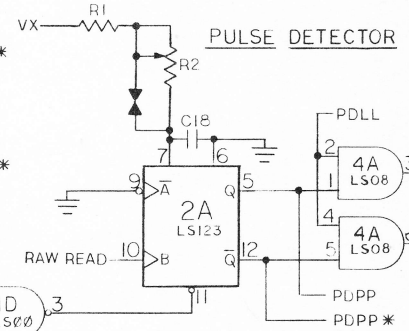
B



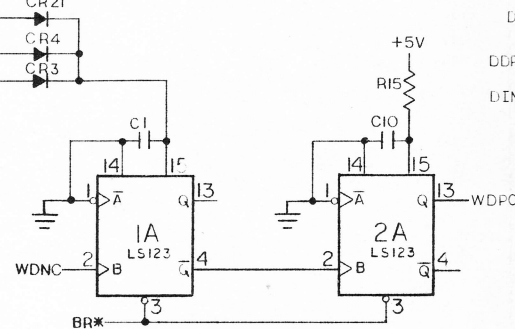
A

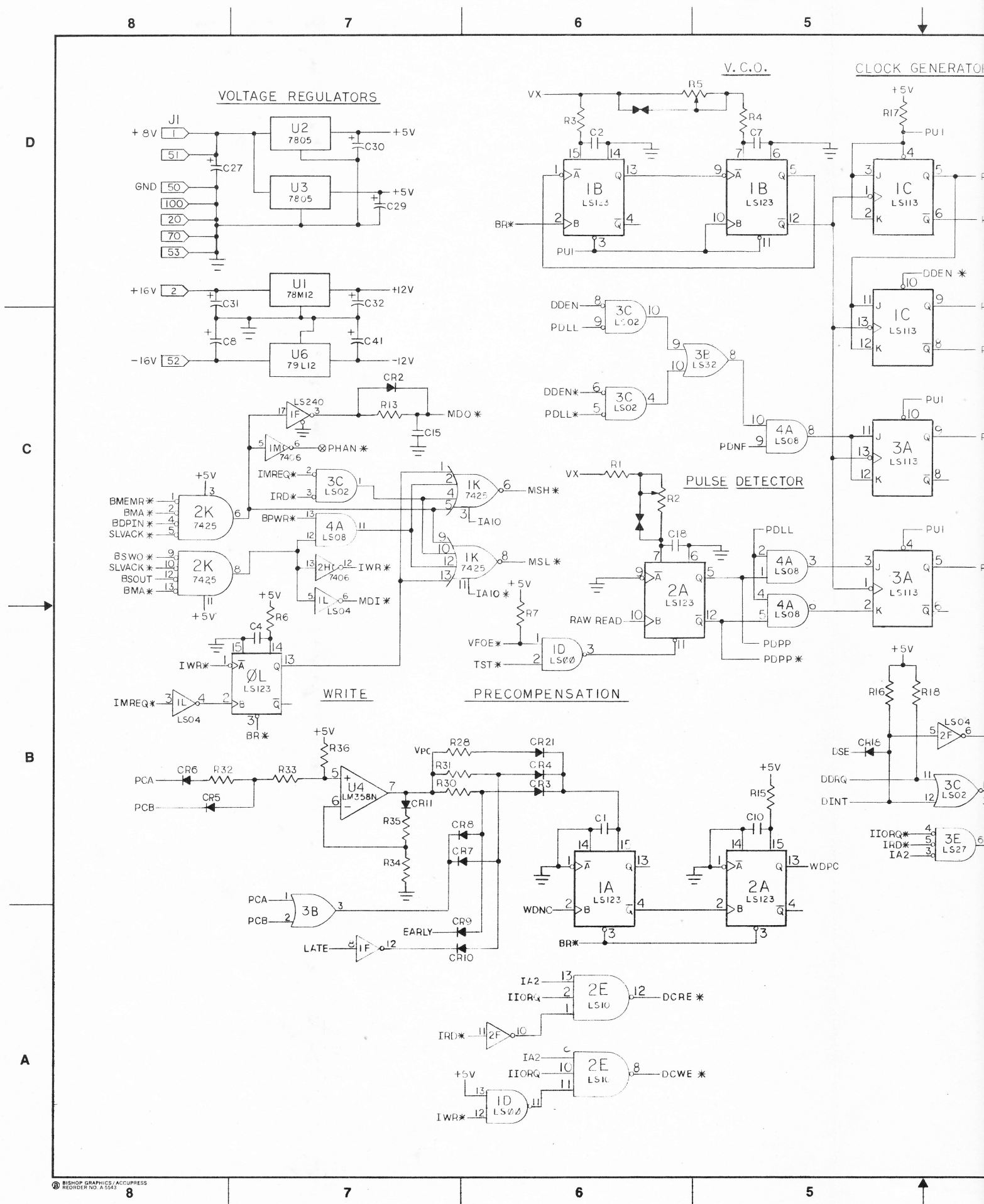


PULSE DETECTOR

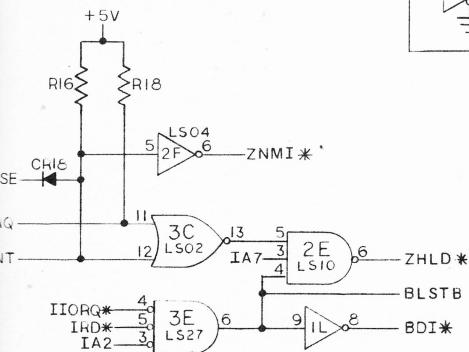
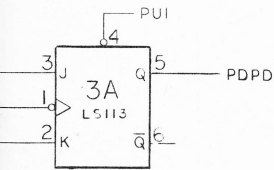
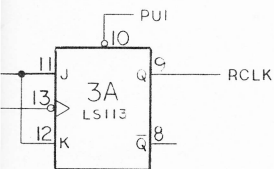
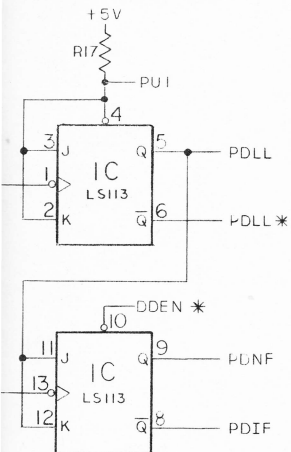


PRECOMPENSATION

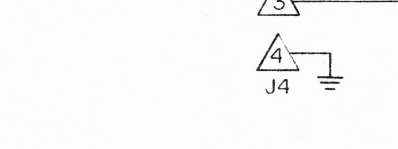
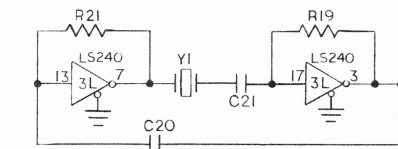
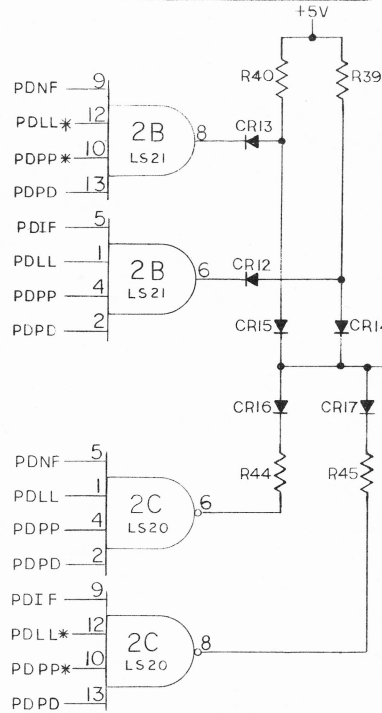




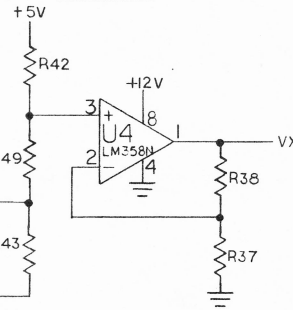
CLOCK GENERATOR



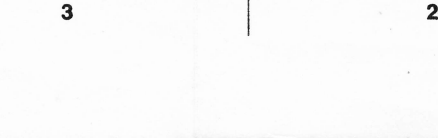
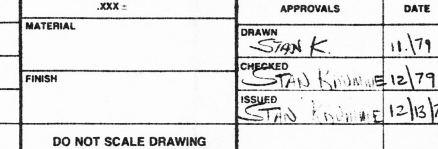
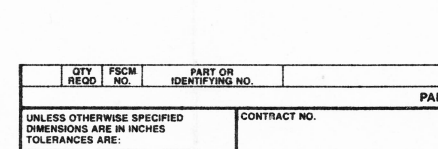
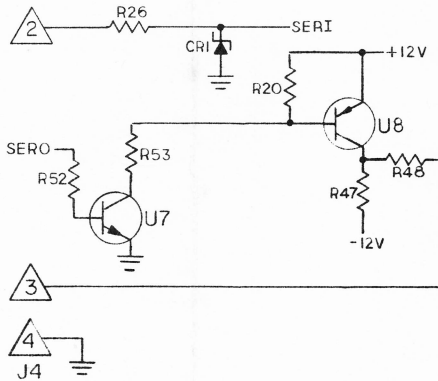
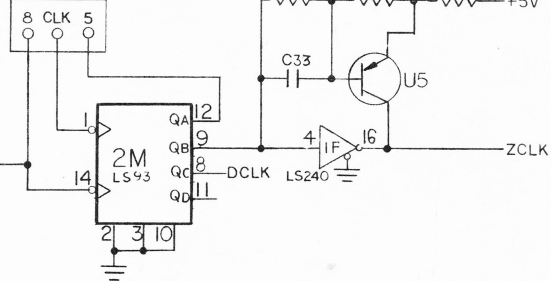
PHASE COMPARATOR



FILTER



CLOCK SELECT



DWG. NO. SH REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
------	------	-------------	------	----------

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:				
FRACTIONS DECIMALS ANGLES				
.XX .XXX .XXX				
MATERIAL				
FINISH				
NEXT ASSY USED ON				
APPLICATION DO NOT SCALE DRAWING				
CONTRACT NO.				
APPROVALS DATE				
DRAWN				
CHECKED				
ISSUED				
SIZE FSCM NO. DWG. NO. REV.				
D IOD-1200 A				
SCALE SHEET 2 OF 2				

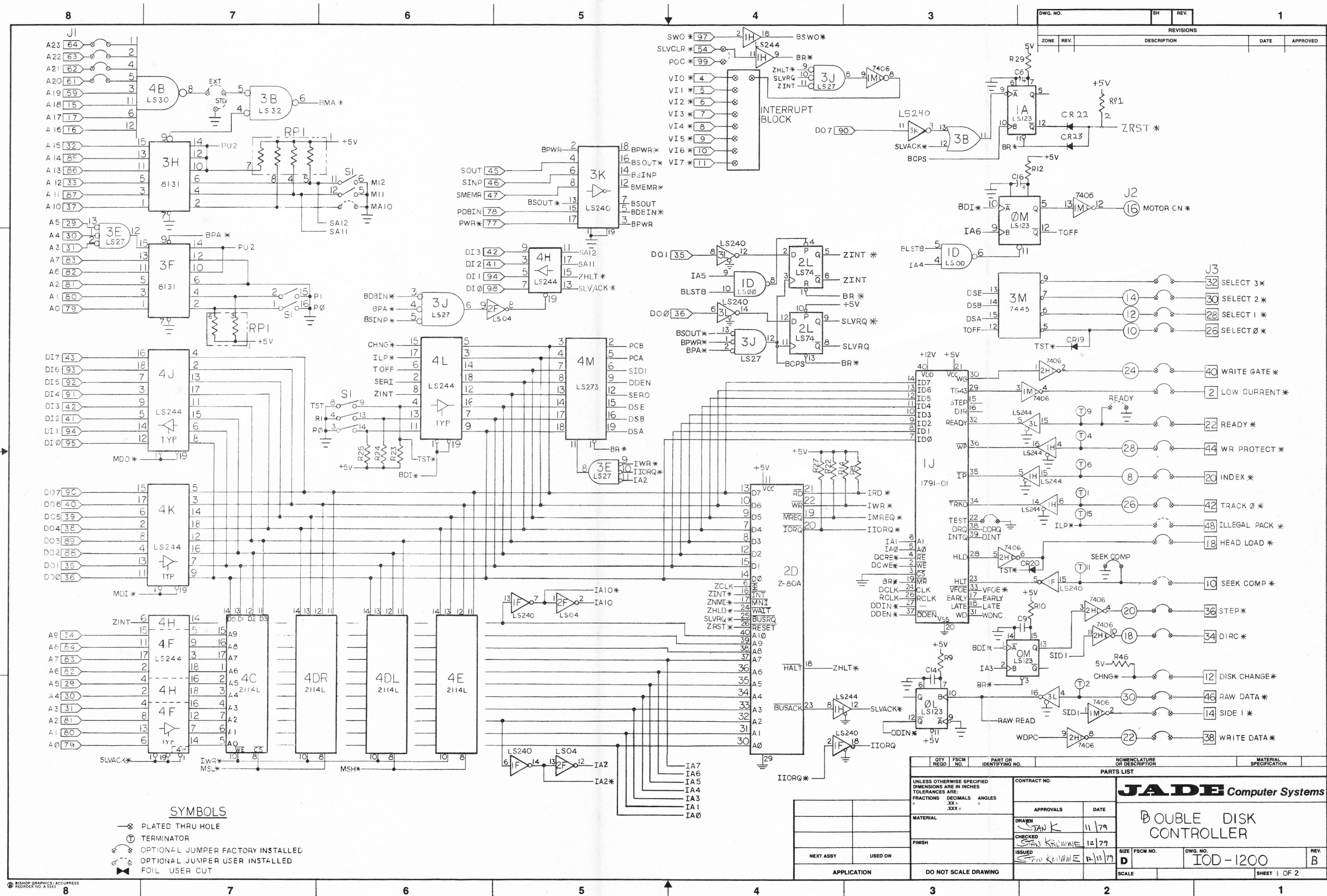
JADE Computer Systems

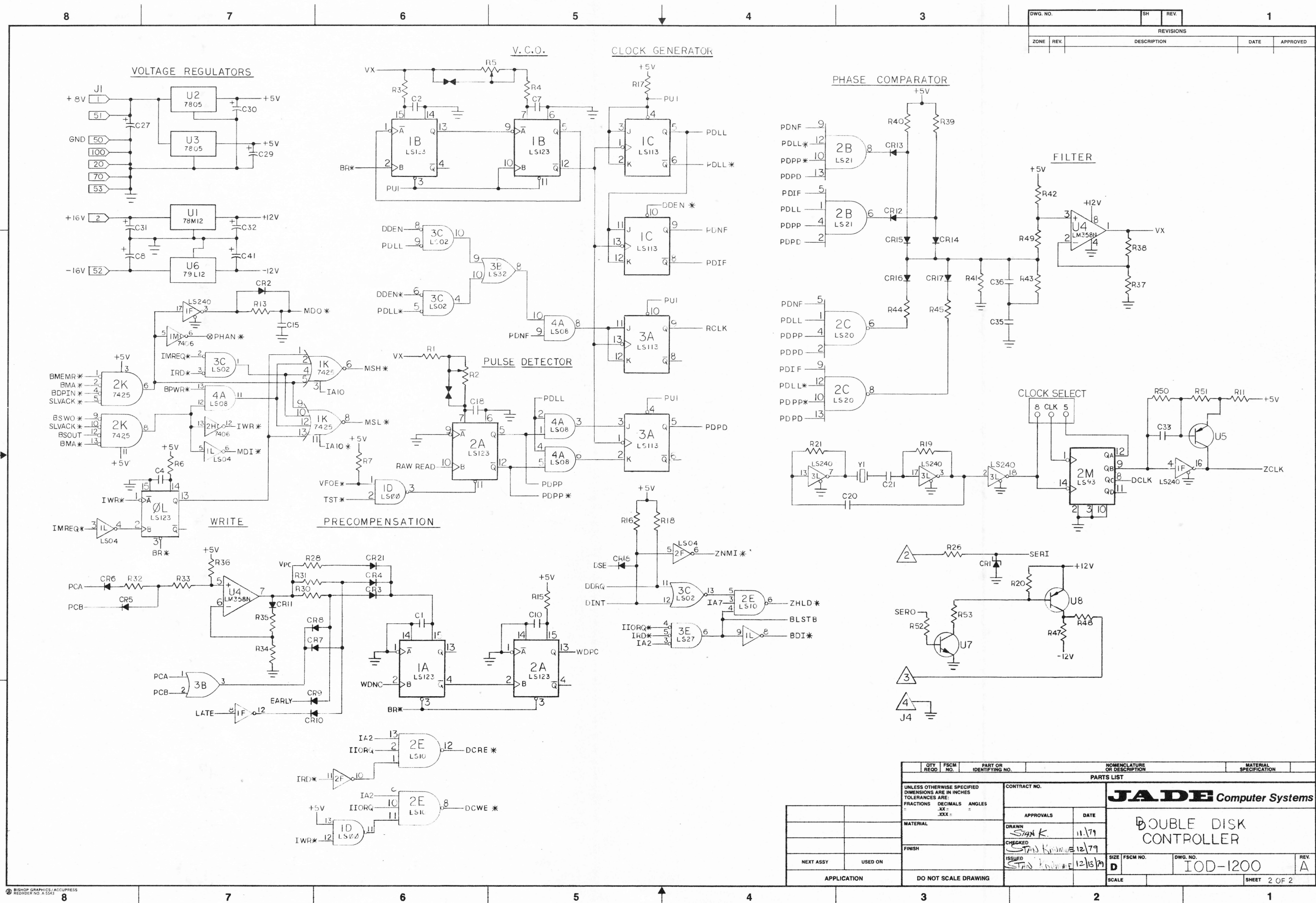
DOUBLE DISK CONTROLLER

SIZE FSCM NO. DWG. NO. REV.

D IOD-1200 A

SCALE SHEET 2 OF 2





DWG. NO.		SH	REV.	1	
ZONE		REV.	DESCRIPTION		DATE
					APPROVED

QTY REQD.		FSCM NO.	PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION	
PARTS LIST									
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX °			CONTRACT NO.		JADE Computer Systems DOUBLE DISK CONTROLLER				
			APPROVALS						DATE
			DRAWN Stan K.						11/79
			CHECKED Stan K.						12/79
MATERIAL			ISSUED Stan K.		12/13/79	SIZE FSCM NO.		DWG. NO.	REV.
FINISH						D		IOD-1200	A
DO NOT SCALE DRAWING						SCALE		SHEET	2 OF 2

SECTION 3

BOARD ASSEMBLY

3.1 INTRODUCTION

If you have purchased the JADE DOUBLE D Disk Controller as a kit, we strongly urge you to read this section in its entirety before attempting to assemble the board. This board is intended for those people who have had some prior experience with digital electronics and circuit board assembly. If you do not, it is highly recommended that you find an experienced person to help you with the assembly of this board.

Although there are about as many ways of assembling a board as the number of components factorial, if you will follow the assembly instructions STEP-BY-STEP, construction will be easier for you and much more pleasurable for both of us. It will help to mark the boxes as you complete each step.

Make sure you have the tools you will need to assemble this kit. For this board you will need the following: a soldering iron (25 watts maximum), ROSIN CORE solder (preferably 63/37), diagonal cutters, a small magnifying glass, a screwdriver, a lead former or a pair of needle-nose pliers, and a small tube of heat sink compound.

3.2 ASSEMBLY

- [] Check the parts received againsts the parts list. Take special care to correctly identify look-alike parts; resistors, capacitors, and diodes. If anything is missing from your kit, please call Jade's Customer Service Department and report the shortage immediately.
- [] USE EYE PROTECTION WHILE SOLDERING OR CUTTING WIRE
- [] When inserting IC sockets be sure to observe the pin 1 notch for proper alignment.
- [] Install 8-pin sockets at U4 and J4. Do not solder yet.
- [] Install 14-pin sockets at 1C, 1D, 1K, 1L, 1M, 2B, 2C, 2E, 2F, 2H, 2K, 2L, 2M, 3A, 3B, 3C, 3E, 3J, 4A, and 4B. Do not solder yet.
- [] Install 16-pin sockets at 0L, 0M, 1A, 1B, 1E, 2A, 3F, 3H, and 3M. Do not solder yet.

- [] Install 18-pin sockets at 4C, 4DL, 4DR, and 4E. Do not solder yet.
- [] Install 20-pin sockets at 1F, 1H, 3K, 3L, 4F, 4H, 4J, 4K, 4L, and 4M. Do not solder yet.
- [] Install 40-pin sockets at 1J and 2D. Do not solder yet.
- [] Place the flat styrofoam cover you recieved with your kit box firmly against the component side of the board. Turn the board over, holding the flat styrofoam piece tightly against the board. Press the board down, forcing the socktes into the styrofoam. Now solder the alternating corner pins of the IC sockets to hold them in place temorarily (pins 8 and 16 on a 16-pin socket, for instance).
- [] Turn the board over and very carefully inspect it to determine that all the IC sockets are down flat against the board. If you find any that are not down flat, melt the solder joints of the IC socket while pressing it down against the board.
- [] Now that all IC sockets are down firmly on the board, turn the board solder side up. Make sure all IC socket pins are sticking through the holes. IC sockets are very hard to remove after they are completely soldered in. Remove any socket not installed properly, straighten the pin and re-insert.
- [] Solder all IC pins.

NOTE: For the following steps the closest IC socket location for each part will be enclosed [IC#].

- [] Solder in the 1N748-750 diode at CR1 (4M).
- [] Solder in one 1N270 diode at CR2 (2L). The polarity shown in the silkscreen is wrong. Install in reverse.
- [] Install six 1N270 diodes at the following locations:
 - [] CR5 (U4) [] CR6 (U4) [] CR7 (1A)
 - [] CR8 (1A) [] CR9 (U4) [] CR10 (U4)

- [] Install two 1N914B diodes at the following locations. ONLY USE THE "B" VERSIONS!
 - [] CR19 (1D) [] CR20 (4L)
- [] Install two 1N914 diodes at the following locations. The polarity of the silkscreen is wrong (SORRY). Install in reverse.
 - [] CR16 (2B) [] CR17 (2B)
- [] Install nine 1N914 diodes at the following locations:

[] CR3 (U4)	[] CR4 (U4)	[] CR11 (U4)
[] CR12 (2A)	[] CR13 (1B)	[] CR14 (U4)
[] CR15 (U4)	[] CR18 (4M)	[] CR21 (1B)
- [] Install the 3.3K ohm 8-pin SIP resistor at RP1 (2F). Be carefull to align pin 1.
- [] Install the 10K ohm trimmers at the following locations:
 - [] R2 [] R5
- [] Be VERY CAREFUL in reading the resistor color codes as there are many different values used in this kit. If needed, use an ohm meter!
- [] Install the 1.0K resistors (Brown-Black-Red) at the following locations:
 - [] R17 (3B) [] R19 (2M) [] R21 (3M)
- [] Install the 4.7K resistors (Yellow-Purple-Red) at the following locations:

[] R8 (3A)	[] R14 (4A)	[] R22 (3B)
[] R23 (4K)	[] R24 (4L)	[] R25 (4M)
[] R27 (3A)	[] R39 (2A)	[] R40 (2A)
- [] Install four 10K resistors (Brown-Black-Orange) at the following locations:
 - [] R7 (4J) [] R16 (3A) [] R18 (3B)
 - [] R36 (U4)
- [] Install the 7.5K resistors (Purple-Green-Red) at the following locations:
 - [] R9 (0L) [] R15 (3A)

- [] Install the 27K resistors (Red-Purple-Orange) at the following locations:
 - [] R20 (1A) [] R32 (1A) [] R38 (2A)
- [] Install the 51K resistors (Green-Brown-Orange) at the following locations:
 - [] R29 (2A) [] R34 (U4)
- [] Install the 30K resistors (Orange-Black-Orange) at the following locations:
 - [] R10 (OM) [] R35 (2A)
- [] Install the 4.3K resistors (Yellow-Orange-Red) at the following locations:
 - [] R44 (2A) [] R45 (2A)
- [] Install the 5.1K resistors (Green-Brown-Red) at the following locations:
 - [] R26 (4L) [] R52 (1A)
- [] Install the 33K resistor (Orange-Orange-Orange) at R28 (1A-1B).
- [] Install the 13K resistor (Brown-Orange-Orange) at R30 (1A).
- [] Install the 22 ohm resistor (Red-Red-Black) at R11 (1K-2K).
- [] Install the 240K resistor (Red-Yellow-Yellow) at R12 (1M).
- [] Install the 300 ohm resistor (Orange-Black-Brown) at R13 (1L-2M).
- [] Install the 22K resistor (Red-Red-Orange) at R33 (1A).
- [] Install the 47K resistor (Yellow-Purple-Orange) at R31 (1A).
- [] Install the 20K resistor (Red-Black-Orange) at R37 (2A).
- [] Install the 470K resistor (Yellow-Purple-Yellow) at R41 (2A).
- [] Install the 390K resistor (Orange-White-Yellow) at R42 (2A).

- [] Install the 2.4K resistor (Red-Yellow-Red) at R43 (2A).
- [] Install the 150 ohm resistor (Brown-Green-Brown) at R46 (4M).
- [] Install the 2.0K resistor (Red-Black-Red) at R47 (U1).
- [] Install the 120 Ohm resistor (Brown-Red-Brown) at R48 (U1).
- [] Install the 82K resistor (Grey-Red-Orange) at R49 (2A).
- [] Install the 220 ohm resistor (Red-Red-Brown) at R51 (1K-1L).
- [] Install the 2.7K resistor (Red-Purple-Red) at R53 (U1).
- [] Install the 0.1 uf capacitors (104) at the following locations:

[] C3 (1C)	[] C5 (OM)	[] C11 (1B)
[] C13 (1E-2E)	[] C17 (2M)	[] C19 (2M)
[] C22 (3A-4A)	[] C26 (4M)	[] C12 (1C)
[] C23 (3C-4C)	[] C24 (3D-4D)	[] C25 (3E)
[] C28 (2C-3C)	[] C34 (U4)	[] C37 (1A)
[] C38 (1A)	[] C39 (1E)	[] C40 (2M)
- [] Install the 25 pf mica capacitors at the following locations:

[] C2 (1B)	[] C4 (OL)	[] C7 (1A)
[] C10 (2A-2B)	[] C14 (OL-OM)	
- [] Install the 200 pf mica capacitors at the following locations:

[] C6 (1A)	[] C9 (1L-1M)	[] C15 (1M)
[] C18 (2A)		
- [] Install the 6.8 uf 35 volt tantalum capacitors at the following locations. Observe polarity!

[] C8 (4A)	[] C31 (4A)
-------------	--------------
- [] Install the 10 uf 10 volt (106) tantalum capacitors at the following locations. Observe polarity!

- [] C29 (4A-4B) [] C30 (3A)
- [] Install the 4.7 uf 25 volt tantalum capacitors at the following locations. Observe polarity!
- [] C32 (U6) [] C41 (4B)
- [] Install the 10 pf mica capacitor at C1 (1A-1B).
- [] Install the 47 uf 6.3 volt tantalum capacitor at C16 (1M). Observe polarity, positive side is toward (0M).
- [] Install 0.022 uf (223) ceramic capacitor at C20 (3K-3L).
- [] Install the 100 pf mica capacitor at C21 (3L-3M).
- [] Install the 22 uf 25 volt tantalum capacitor at C27 (U3). Observe polarity!
- [] Select the 33 pf mica capacitor and the 1.2K resistor (Brown-Red-Red). The capacitor is to be mounted on top of the resistor, and not to be inserted at C33. The resistor is to be inserted at R54 with the capacitor connected across the resistor leads (parallel). Observe positioning of parts before soldering, for a good fit.
- [] Install the 0.01 uf ceramic capacitor at C35 (U4).
- [] Install the 1000 pf mica capacitor at C36 (U4).
- [] Install the 78M12 regulator at U1 (1A). Leave an 1/8" gap between it and the PCB.
- [] Install the 7805 regulators at U2 and U3 (3A-4A) using the heat sinks and the #6 hardware. A small file should be used on the U2 heat sink where it comes close to C34, as a small plated-thru-hole located there can cause a short.
- Use the needle-nose pliers to bend the leads of the 7805s before mounting. Mount the regulators on the heat sinks with the hardware provided, then solder.
- [] Install the 2N2907A transistors at U5 and U8. Leave an 1/8" gap between the transistors and the PCB.
- [] Install the 2N2222A transistor at U7. Leave an 1/8" gap between it and the PCB.

- [] Install the 79L12 regulator at U6 (4B). Align part as shown in silkscreen.
- [] Install the 8.000 Mhz xtal at Y1 (3L).
- [] Install switch at S1 (3F-3H).

- [] Insert the DOUBLE D controller card into an S100 mainframe. Turn on the power switch and check the following voltages.
 - [] U2 has +5 volt output.
 - [] U3 has +5 volt output.
 - [] U1 has +12 volt output.
 - [] U6 has -5 volt output.

- [] THE FOLLOWING STEPS ARE FOR 8" DRIVES.
 - [] Install a 10K resistor (Brown-Black-Orange) at R1 (1A).
 - [] Install a 15K resistor (Brown-Green-Orange) at R3 (1A).
 - [] Install a 10K resistor (Brown-Black-Orange) at R4 (1A).
 - [] Install a 6.2K resistor (Blue-Red-Red) at R6 (OL).
 - [] Install a jumper wire from "CLK" to "8" in the CLOCK SELECT BLOCK near ICs 2L-2M.

- [] THE FOLLOWING STEPS ARE FOR 5" DRIVES.
 - [] Install a 24K resistor (Red-Yellow-Orange) at R1 (1A).
 - [] Install a 39K resistor (Orange-White-Orange) at R3 (1A).
 - [] Install a 36K resistor (Orange-Blue-Orange) at R4 (1A).
 - [] Install an 8.2K resistor (Grey-Red-Orange) at R6 (OL).
 - [] Install a jumper wire from "CLK" to "5" in the CLOCK SELECT BLOCK near ICs 2L-2M.

- [] For use with a 16 bit address bus install a jumper from "M" to "S" in the ADDRESS MODE JUMPER BLOCK. In this mode IC 4B is not needed.

- [] For Use with a 24 bit address bus install a jumper from "M" to "E" in the ADDRESS MODE JUMPER BLOCK. In this mode IC 4B is required.

- [] Insert the LM358 at U4.

- [] Insert the 74LS00 IC at 1D.
- [] Insert the 74LS02 IC at 3C.
- [] Insert the 74LS04 ICs at 1L and 2F.
- [] Insert the 7406 ICs at 1M and 2H.
- [] Insert the 74LS08 IC at 4A.
- [] Insert the 74LS10 IC at 2E.
- [] Insert the 74LS20 IC at 2C.
- [] Insert the 74LS21 IC at 2B.
- [] Insert the 74LS27 ICs at 3E and 3J.
- [] Insert the 74LS32 IC at 3B.
- [] Insert the 74LS74 IC at 2L.
- [] Insert the 74LS93 IC at 2M.
- [] Insert the 74LS113 ICs at 1C and 3A.
- [] Insert the 74LS123 ICs at 1A, 1B, 2A, 0L, and 0M.
- [] Insert the 74LS240 ICs at 1F, 3K, and 3L.
- [] Insert the 74LS244 ICs at 1H, 4F, 4H, 4J, 4K, and 4L.
- [] Insert the 74LS273 IC at 4M.
- [] Insert the 7425 ICs at 1k and 2K.
- [] Insert the 7445 IC at 3M.
- [] Insert the 8131 ICs at 3F and 3H.
- [] Insert the 16-pin 150 ohm resistor pack at 1E.
- [] Insert the Z80A microprocessor at 2D.
- [] Insert the WD-1791-01 controller at 1J.
- [] Insert the 21141-3 static rams at 4C, 4DL, 4DR, and 4E.
- [] Inspect all inserted ICs for bent pins.
- [] Place DOUBLE D controller board in an extender board in an S100 mainframe. Open all switches in

S1. Turn power switch on.

- [] Adjust trimmer R5 for a 2.0 mhz clock signal at IC 1B pin 12. (1.0 mhz for 5" configuration)
- [] Turn power switch off. Connect disk interface cable from controller to the disk drive. Observe pin 1 indications. Turn power switch on.
- [] Insert a preformatted single density diskette into the drive (DRIVE 0) and close the door.
- [] Close switch TST*. This will select drive 0, turn the motor control on, and load the head.
- [] Adjust R2 for a 1.0 us output from one-shot 2A pin 5. (2.0 us output on 5" configuration)
- [] Open switch TST*. Turn power switch off.

APPENDIX B

PARTS LIST

<u>RESISTORS</u>		<u>LOCATION-IC</u>		
R1-8"	10K	1/4W	5%	1A
5"	24K	1/4w	5%	
R2	10K	Trimmer		1A
	BOURNS	3006P-1-103		
R3-8"	15K	1/4W	5%	1A
5"	39K	1/4w	5%	
R4-8"	10K	1/4W	5%	1A
5"	36K	1/4w	5%	
R5	10K	Trimmer		1A
	BOURNS	3006P-1-103		
R6-8"	6.2K	1/4W	5%	OL
5"	8.2k	1/4w	5%	
R7	10K	1/4W	5%	4J-4K
R8	4.7K	1/4W	5%	3A
R9	7.5K	1/4W	5%	OL-1L
R10	30K	1/4W	5%	OM-1M
R11	22 OHM	1/4W	5%	1K-2K
R12	240K	1/4W	5%	1M
R13	300 OHM	1/4W	5%	1L-2M
R14	4.7K	1/4W	5%	4A-4B
R15	7.5K	1/4W	5%	3A-3B
R16	10K	1/4W	5%	3A-3B
R17	1.0K	1/4W	5%	3B-3C
R18	10K	1/4W	5%	3B-3C
R19	1.0K	1/4W	5%	2M-3M
R20	27K	1/4W	5%	U1
R21	1.0K	1/4K	5%	3M
R22	4.7K	1/4W	5%	3B
R23	4.7K	1/4W	5%	4K-4L
R24	4.7K	1/4W	5%	4L-4M
R25	4.7K	1/4W	5%	4M
R26	5.1K	1/4W	5%	4L
R27	4.7K	1/4W	5%	3A-3B
R28	33K	1/4W	5%	1A-1B
R29	51K	1/4W	5%	2A
R30	13K	1/4W	5%	1A
R31	47K	1/4W	5%	1A
R32	27K	1/4W	5%	1A
R33	22K	1/4W	5%	1A
R34	51K	1/4W	5%	2A

R35	30K	1/4W	5%	2A
R36	10K	1/4W	5%	2A
R37	20K	1/4W	5%	2A
R38	27K	1/4W	5%	2A
R39	4.7K	1/4W	5%	2A
R40	4.7K	1/4W	5%	2A
R41	470K	1/4W	5%	2A
R42	390K	1/4W	5%	2A
R43	2.4K	1/4W	5%	2A
R44	4.3K	1/4W	5%	2A
R45	4.3K	1/4W	5%	2A
R46	150 OHM	1/4W	5%	4M
R47	2.0K	1/4W	5%	U1
R48	120 OHM	1/4W	5%	U1
R49	82K	1/4W	5%	2A
R50	1.2K	1/4W	5%	1K-1L
R51	220 OHM	1/4W	5%	1K-1L
R52	5.1K	1/4W	5%	1A
R53	2.7K	1/4W	5%	U1

RP1 8 PIN SIP 3.3K

(1E) BOURNS 4116R-151
 16 PIN 15 RESISTOR
 150 OHMS, OR EQV.

DIODES

CR1 1N748-1N750

CR2, CR5, CR6, CR7
 CR8, CR9, CR10, CR22
 CR23

1N270

CR3, CR4, CR11, CR12
 CR13, CR14, CR15, CR16
 CR17, CR18, CR21

1N914, 1N4148, OR EQV

CR19, CR20

1N914B, 1N4448, OR EQV

CAPACITORSLOCATIONS

C1	10 PF 5% MICA	1A-1B
C2	25 PF 5% MICA	1B
C3	0.1 UF MONOLYTHIC	1C
C4	25 PF 5% MICA	OL
C5	0.1 UF MONOLYTHIC	OM
C6	200 PF 5% MICA	1A
C7	25 PF 5% MICA	1A-1B
C8	6.8 UF 35V DIPPED TANT.	4A
C9	200 PF 5% MICA	1L-1M
C10	25 PF 5% MICA	2A-2B
C11	0.1 UF MONOLYTHIC	1B-2B
C12	0.1 UF MONOLYTHIC	1C-2C
C13	0.1 UF MONOLYTHIC	1E-2E
C14	25 PF 5% MICA	OL-OM
C15	200 PF 5% MICA	1M
C16	47 UF 6.3V DIPPED TANT.	1M
C17	0.1 UF MONOLYTHIC	2M
C18	200 PF 5% MICA	2A
C19	0.1 UF MONOLYTHIC	2M
C20	0.022 UF CERAMIC 10%	3K-3L
C21	100 PF 5% MICA	3L-3M
C22	0.1 UF MONOLYTHIC	3A-4A
C23	0.1 UF MONOLYTHIC	3C-4C
C24	0.1 UF MONOLYTHIC	3D-4D
C25	0.1 UF MONOLYTHIC	3E-4E
C26	0.1 UF MONOLYTHIC	4M
C27	22 UF 25V DIPPED TANT.	U3
C28	0.1 UF MONOLYTHIC	2C-3C
C29	10 UF 10V DIPPED TANT.	4A-4B
C30	10 UF 10V DIPPED TANT	3A
C31	6.8 UF 35V DIPPED TANT.	4A
C32	4.7 UF 25V DIPPED TANT.	U6
C33	33 PF 5% MICA	1K-1L
C34	0.1 UF MONOLYTHIC	U4
C35	0.01 UF 10% CERAMIC	U4
C36	1000 PF MICA 5%	U4
C37	0.1 UF MONOLYTHIC	1A-2A
C38	0.1 UF MONOLYTHIC	1A
C39	0.1 UF MONOLYTHIC	1E
C40	0.1 UF MONOLYTHIC	2M
C41	4.7 UF 25V DIPPED TANT.	4B

MISCELLANEOUS

1 EA	8 POSITION DIP SWITCH
2 EA	AHAM-TOR #372-A HEAT SINK
2 EA	#6 SCREW, NUT, AND WASHER
1 EA	8.000 MHZ XTAL, Y1
1 EA	8 PIN DIP PLUG AND COVER

DIGITAL CIRCUITS

(1A)	74LS123	(2A)	74LS123	(3A)	74LS113	(4A)	74LS08
(1B)	74LS123	(2B)	74LS21	(3B)	74LS32	(4B)	74LS30
(1C)	74LS113	(2C)	74LS20	(3C)	74LS02	(4C)	2114-3L
(1D)	74LS00	(2D)	Z80A			(4DL)	2114-3L
						(4DR)	2114-3L
(1E)	RES-PK	(2E)	74LS10	(3E)	74LS27	(4E)	2114-3L
(1F)	74LS240	(2F)	74LS04	(3F)	8131	(4F)	74LS244
(1H)	74LS244	(2H)	7406	(3H)	8131	(4H)	74LS244
(1J)	1791-01			(3J)	74LS27	(4J)	74LS244
(1K)	7425	(2K)	7425	(3K)	74LS240	(4K)	74LS244
(1L)	74LS04	(2L)	74LS74	(3L)	74LS240	(4L)	74LS244
(1M)	7406	(2M)	74LS93	(3M)	7445	(4M)	74LS273
(OL)	74LS123	(OM)	74LS123				

ANALOG CIRCUITS

(U1)	78M12	(TO-5)
(U2)	7805	(TO-220)
(U3)	7805	(TO-220)
(U4)	LM358	(8-PIN DIP)
(U5)	2N2907	(TO-18)
(U6)	79L12	(TO-92)
(U7)	2N2222	(TO-18)
(U8)	2N2907	(TO-18)

SOCKETS

8 PIN DIP SOCKET	2 EA
14 PIN DIP SOCKET	20 EA
16 PIN DIP SOCKET	9 EA
18 PIN DIP SOCKET	4 EA
20 PIN DIP SOCKET	10 EA
40 PIN DIP SOCKET	2 EA

APPENDIX C

INTERNAL SIGNAL DEFINITIONS

BCPS	BOARD - CONTROL PORT STROBE
BDBIN	BUS - DATA BUS IN
BDI*	BOARD - DATA IN
BLSTB	BOARD - FUNCTION STROBE
BMA*	BOARD - MEMORY ADDRESSED
BMA	BOARD - PORT ADDRESSED
BMEMR	BUS - MEMORY READ
BR*	BOARD - RESET
BPWR	BUS - PROCESSOR WRITE
BSINP	BUS - STATUS INPUT
BSOUT	BUS STATUS OUTPUT
BSWO	BUS STATUS WRITE OUT
CHNG*	DISK CHANGED
DCLK	1791-01 CLOCK
DCRE*	1791-01 READ ENABLE
DCWE*	1791-01 WRITE ENABLE
DDEN	DOUBLE DENSITY ENABLE
DDIN*	1791-01 DISK DATA IN
DDRQ	1791-01 DATA REQUEST
DINT	1791-01 INTERRUPT REQ
DSA	DRIVE SELECT A
DSB	DRIVE SELECT B
DSE	DRIVE SELECT ENABLE
IAnn	INTERNAL ADDRESS BIT nn
IIORQ*	INTERNAL Z80A I/O REQ
ILP*	ILLEGAL PACK
IMREQ*	INTERNAL Z80A MEM REQ
IRD*	INTERNAL Z80A READ CYCLE
IWR*	INTERNAL Z80A WRITE CYCLE
MDI*	MEMORY DATA IN
MDO*	MEMORY DATA OUT
MSH*	MEMORY SELECT HIGH
MSL*	MEMORY SELECT LOW
PCA	PRECOMP SELECT A
PCB	PRECOMP SELECT B
PDIF	PHASE DETECT ILLEGAL FRAME
PDLL	PHASE DETECT LEAD/LAG
PDNF	PHASE DETECT NORMAL FRAME
PDPD	PHASE DETECT PULSE DETECTED
PDPP	PHASE DETECT PULSE PRESENT

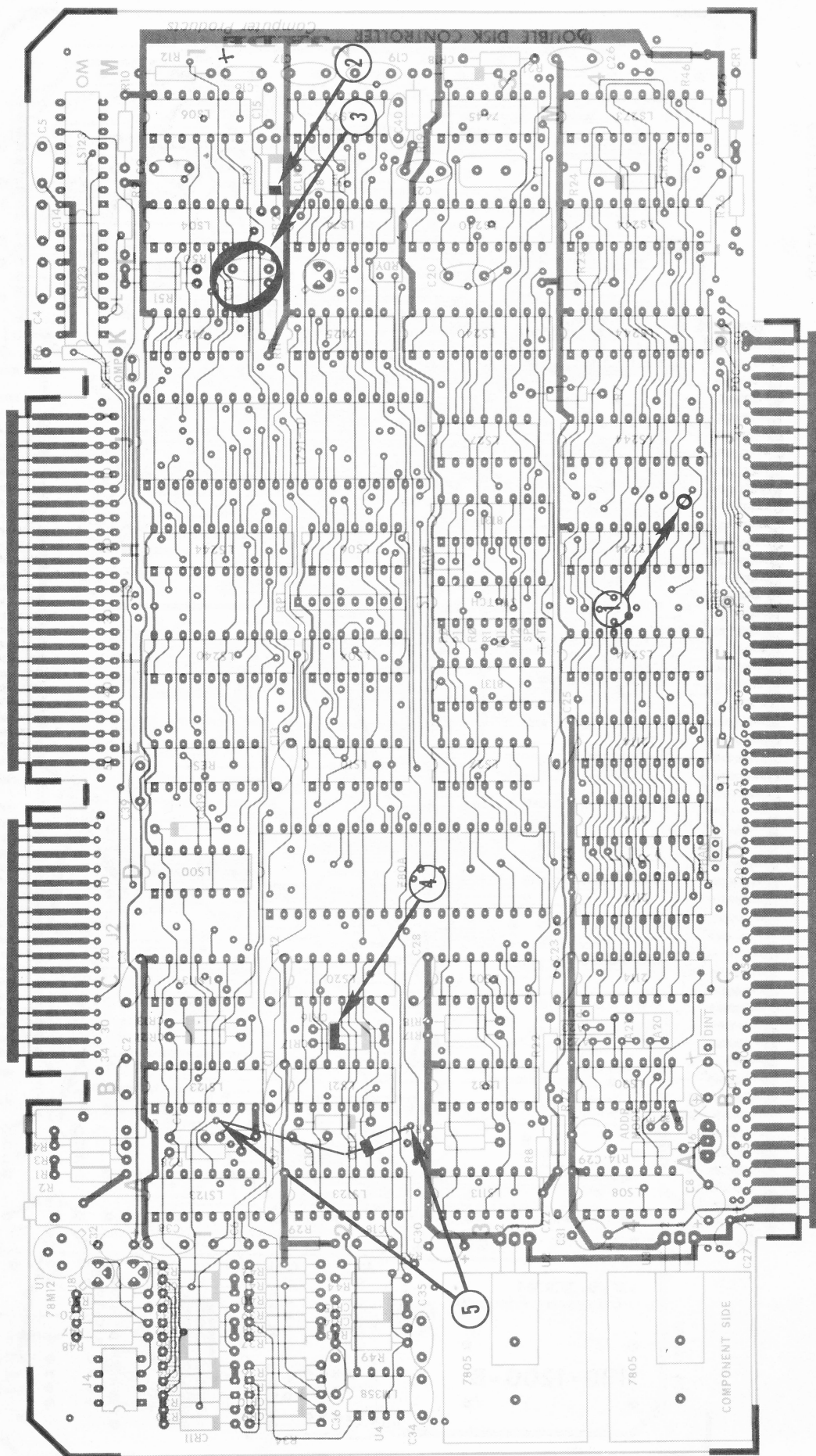
RCLK	1791-01 READ WINDOW
SA11	ADDRESS SWITCH M11
SA12	ADDRESS SWITCH M12
SERI	TTL LEVEL OF EIA IN
SERO	TTL LEVEL OF EIA OUT
SID1	SIDE 1 SELECT
SLVACK*	MEM TRANSFER ACK
SLVREQ*	MEM TRANSFER REQ
TOFF	TIMER OFF
TST*	TEST PLL
VFOE*	PHASE LOCK LOOP ENABLE
VPC	PRECOMP INTENSITY
VX	LOOP OSC VOLTAGE
WDNC	WRITE DATA NOT COMPENSATED
WDPC	WRITE DATA PRECOMPENSATED
ZCLK	Z80A CLOCK
ZHLD*	Z80A WAIT REQUEST
ZINT*	Z80A INTERRUPT REQ
ZNMI*	Z80A N.M. INTERRUPT REQ
ZRST*	Z80A RESET

APPENDIX D

S-100 BUS CONNECTIONS

PIN #	SIGNAL	FUNCTION	PIN#	SIGNAL	FUNCTION
1	+8 volts	Power	51	+8 VOLTS	Power
2	+16 volts	Power	52	-16 VOLTS	Power
4	VI0*	Interrupt	53	GND	Ground
5	VI1*	Interrupt	54	SLAVE CLR*	A Reset
6	VI2*	Interrupt	59	A19	Extd Addr
7	VI3*	Interrupt	61	A20	Extd Addr
8	VI4*	Interrupt	62	A21	Extd Addr
9	VI5*	Interrupt	63	A22	Extd Addr
10	VI6*	Interrupt	64	A23	Extd Addr
11	VI7*	Interrupt	67	PHANTOM*	Dsble Slaves
15	A18	Ext Addr	70	GND	Ground
16	A16	Ext Addr	77	pWR	Processor Sig
17	A17	Ext Addr	78	pDBIN	Processor Sig
20	GND	Ground	79	A0	Address 0
29	A5	Address 5	80	A1	Address 1
30	A4	Address 4	81	A2	Address 2
31	A3	Address 3	82	A6	Address 6
32	A15	Address 15	83	A7	Address 7
33	A12	Address 12	84	A8	Address 8
34	A9	Address 9	85	A13	Address 13
35	DO1	Data Out 1	86	A14	Address 14
36	DO0	Data Out 0	87	A11	Address 11
37	A10	Address 10	88	DO2	Data Out 2
38	DO4	Data Out 4	89	DO3	Data Out 3
39	DO5	Data Out 5	90	DO7	Data Out 7
40	DO6	Data Out 6	91	DI4	Data In 4
41	DI2	Data In 2	92	DI5	Data In 5
42	DI3	Data In 3	93	DI6	Data In 6
43	DI7	Data In 7	94	DI1	Data In 1
45	sOUT	Status Out	95	DIO	Data In 0
46	sIN	Status In	97	sWO	Write Out
47	sMEMR	Stat Mem Rd	99	POC*	Power On Rst
50	GND	Ground	100	GND	Ground

Date		Description		Amount	
1901	Jan 1	Balance		100.00	
	Jan 15	Received from A. B.		50.00	
	Feb 1	Received from C. D.		25.00	
	Feb 15	Received from E. F.		75.00	
	Mar 1	Received from G. H.		100.00	
	Mar 15	Received from I. J.		50.00	
	Apr 1	Received from K. L.		25.00	
	Apr 15	Received from M. N.		75.00	
	May 1	Received from O. P.		100.00	
	May 15	Received from Q. R.		50.00	
	Jun 1	Received from S. T.		25.00	
	Jun 15	Received from U. V.		75.00	
	Jul 1	Received from W. X.		100.00	
	Jul 15	Received from Y. Z.		50.00	
	Aug 1	Received from A. B.		25.00	
	Aug 15	Received from C. D.		75.00	
	Sep 1	Received from E. F.		100.00	
	Sep 15	Received from G. H.		50.00	
	Oct 1	Received from I. J.		25.00	
	Oct 15	Received from K. L.		75.00	
	Nov 1	Received from M. N.		100.00	
	Nov 15	Received from O. P.		50.00	
	Dec 1	Received from Q. R.		25.00	
	Dec 15	Received from S. T.		75.00	
	Total			1000.00	



Make the following modifications to the DOUBLE D controller board.

COMPONENT SIDE

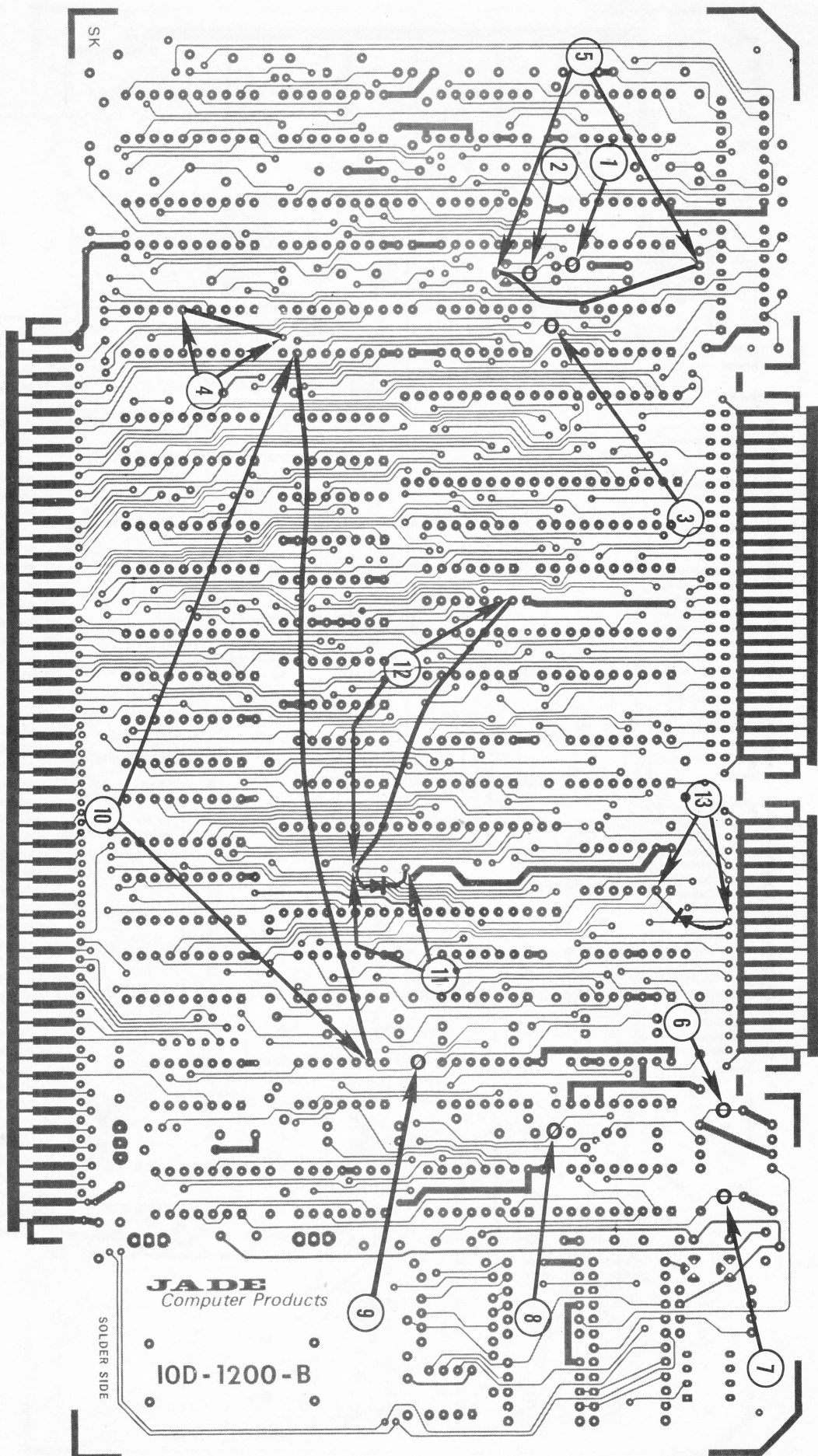
- | | | | |
|-----|--|-----|--|
| [] | 1. CUT foil to IC 4H pin 8 as shown. | [] | 4. NOTE: Diode CR16 and CR17 are shown reversed. |
| [] | 2. NOTE: Diode CR2 is shown reversed. | [] | 5. CR22 (1N270) must be installed as shown. Use a jumper wire on one lead. |
| [] | 3. C33 must be mounted on top of R50. Connect the part in parallel with R50 leads. | | |

change polarity of C4

SOLDER SIDE

1. CUT foil as shown.
2. CUT foil as shown.
3. CUT foil as shown.
4. Install jumper as shown.
5. Install jumper as shown.
6. CUT foil as shown (R5).

7. CUT foil as shown (R2).
8. CUT foil as shown.
9. CUT foil as shown.
10. Install jumper as shown.
11. Install CR23 as shown.
12. Install jumper as shown.
13. Install 1N914B diode as shown.



JADE would welcome your comments about this board. We are very much interested in you, our customer, and we want to provide ourselves with some feedback about how you like the product and documentation. Please take a moment and fill out the questionnaire and return it to us at the address below.

JADE COMPUTER PRODUCTS
TECHNICAL SUPPORT GROUP
4901 WEST ROSECRANS
HAWTHORNE, CA 90250

1. Was your DOUBLE D damaged in shipment? YES NO

2. Were any parts missing? YES NO

If yes, what were they? _____

3. Was the quality of the material and workmanship good? YES NO

4. Did you have any trouble understanding the manual? YES NO

If yes, in what area(s)? _____

5. Have you encountered problems with the DOUBLE D? YES NO

If yes, what? _____

6. Did you solve the problem? YES NO

If yes, how? _____

7. Are you satisfied with your DOUBLE D? YES NO

If not, why? _____

SEE OTHER SIDE

8. Do you have any suggestions for design improvement? YES NO

If yes, what? _____

9. In your opinion, what are the advantages and

disadvantages of the DOUBLE D? _____

10. Other comments? _____

11. NAME: _____

ADDRESS: _____

CITY, STATE: _____

ZIP CODE: _____

PHONE: _____

THANK YOU